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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital sections and digital line system – Access networks

Single-pair high-speed digital subscriber line (SHDSL) transceivers

ITU-T Recommendation G.991.2

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ITU-T Recommendation G.991.2

Single-pair high-speed digital subscriber line (SHDSL) transceivers

Summary

This Recommendation describes a transmission method for data transport in telecommunications access networks. SHDSL transceivers are designed primarily for duplex operation over mixed gauge two-wire twisted metallic pairs. Optional multi-pair operation is supported for extended reach applications. Optional signal regenerators for both single-pair and multi-pair operation are specified, as well. SHDSL transceivers are capable of supporting selected symmetric user data rates in the range of 192 kbit/s to 2312 kbit/s using a Trellis Coded Pulse Amplitude Modulation (TCPAM) line code. Optional extensions described in Annex F allow user data rates up to 5696 kbit/s. SHDSL transceivers are designed to be spectrally compatible with other transmission technologies deployed in the access network, including other DSL technologies. SHDSL transceivers do not support the use of analogue splitting technology for coexistence with either POTS or ISDN. Regional requirements, including both operational differences and performance requirements, are specified in Annexes A, B and C. Requirements for signal regenerators are specified in Annex D. Annex E describes application-specific framing modes that may be supported by SHDSL transceivers.

See Annex H/G.992.1 [1] for specifications of transceivers for use in networks with existing TCM-ISDN service (as specified in Appendix III/G.961, in Bibliography [B1]).

History

With respect to the previous version 1 (2001), this version 2 introduces the following additions and modifications:

- The optional four-wire mode has been extended to a more general multi-pair mode which provides optional support for up to four-pair connections. See 7.2.1.5. Note that the integrity of the optional 4-wire mode in revision 1 is preserved. The four-wire mode is identical to M-pair mode with $M = 2$, except for the method of assigning ordinal numbers to the wire pairs. In four-wire mode, the ordinal numbers (the wire pair identification number) are assigned as described in 6.3, while in M-pair mode the ordinal numbers are assigned to wire pairs as described in 7.2.1.5.
- The loops and test conditions specified in Annex B have been updated (see B.3.3), and Appendix IV, Tabulation of Annex B Noise Profiles, has been added.
- Optional extensions, described in Annex F, allow user data rates up to 5696 kbit/s.
- Deactivation and warm-start, as specified in Annex H, have been added.
- Support for Dynamic Rate Repartitioning has been added to Dual-Bearer mode. See E.10.3.
- TPS-TC definitions have been added for Packet Transfer Mode (E.11), Synchronous Transfer Mode with a Dedicated Signalling Channel (E.12), and V5 Encapsulated ISDN or POTS (E.13).

Source

ITU-T Recommendation G.991.2 was approved on 14 December 2003 by ITU-T Study Group 15 (2001-2004) under the ITU-T Recommendation A.8 procedure.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure e.g. interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

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ITU-T Recommendation G.991.2

Single-pair high-speed digital subscriber line (SHDSL) transceivers

1 Scope

This Recommendation describes a transmission method for providing Single-pair High-speed Digital Subscriber Line (SHDSL) service as a means for data transport in telecommunications access networks. This Recommendation does not specify all the requirements for the implementation of SHDSL transceivers. Rather, it serves only to describe the functionality needed to assure interoperability of equipment from various manufacturers. The definitions of physical user interfaces and other implementation-specific characteristics are beyond the scope of this Recommendation.

For interrelationships of this Recommendation with other G.99x-series ITU-T Recommendations, see ITU-T Rec. G.995.1 in Bibliography [B2] (informative).

The principal characteristics of this Recommendation are as follows:

– provisions for duplex operation over one (or, optionally, multiple) mixed gauge two-wire twisted metallic pairs;
– specification of the physical layer functionality, e.g., line codes and forward error correction;
– specification of the data link layer functionality, e.g., frame synchronization and framing of application, as well as Operations, Administration and Maintenance (OAM) data;
– provisions for optional use of repeaters for extended reach;
– provisions for spectral compatibility with other transmission technologies deployed in the access network;
– provisions for regional requirements, including functional differences and performance requirements.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[1] ITU-T Recommendation G.992.1 (1999), *Asymmetric Digital Subscriber Line (ADSL) transceivers*.

[2] ITU-T Recommendation G.994.1 (2003), *Handshake procedures for digital subscriber line (DSL) transceivers, plus Amendment 1 (2004)*.

[3] ITU-T Recommendation G.997.1 (2003), *Physical layer management for digital subscriber line (DSL) transceivers*.

[4] IETF RFC 1662 (1994), *PPP in HDLC-like Framing*.

[5] ISO 8601:2000, *Data elements and interchange formats – Information interchange – Representation of dates and times*.

[6] ITU-T Recommendation G.996.1 (2001), *Test procedures for Digital Subscriber Line (DSL) transceivers*.

[7] IEC 60950 (1999), *Information technology equipment – Safety*.

[8] ITU-T Recommendation I.432.1 (1999), *B-ISDN user-network interface – Physical layer specification: General characteristics*.

[9] ETSI EN 300 324-1 (1994), *V Interfaces at the digital Local Exchange (LE); V5.1 interface for the support of Access Network (AN); Part 1: V5.1 Interface specification*.

[10] ETSI EG 201 900-1 V1.1.1 (2001), *Services and Protocols for Advanced Networks (SPAN); Narrowband Services over ATM; Loop Emulation Service (LES) using AAL2; Part 1: LES interface specification [ATM Forum Specification af-vmoa-0145.000 (2000), modified]*.

[11] Coded Identification of Equipment Entities of the North American Telecommunications System for Information Exchange [Revision of T1.213-1990 (R1996)], May 2001.

3 Definitions and abbreviations

3.1 Definitions

This Recommendation defines the following terms:

3.1.1 bit-error ratio: The ratio of the number of bits in error to the number of bits sent over a period of time.

3.1.2 downstream: STU-C to STU-R direction (central office to remote terminal).

3.1.3 loopback: A reversal in the direction of the payload (i.e., the user data) at a specified SHDSL network element.

3.1.4 mapper: A device for associating a grouping of bits with a transmission symbol.

3.1.5 micro-interruption: A temporary line interruption.

3.1.6 modulo: A device having limited value outputs (not the same as the mathematical modulo operation).

3.1.7 payload block: One of the sections of a frame containing user data.

3.1.8 plesiochronous: A clocking scheme in which the SHDSL frame is based on the input transmit clock but the symbol clock is based on another independent clock source.

3.1.9 precoder: A device in the transmitter for equalizing some of the channel impairments.

3.1.10 precoder coefficients: Coefficients of the filter in the precoder that are generated in the receiver and transferred to the transmitter.

3.1.11 remote terminal: A terminal located downstream from a central office switching system.

3.1.12 scrambler: A device to randomize a data stream.

3.1.13 segment: The portion of a span between two terminations (either STUs or SRUs).

3.1.14 SHDSL network element: An STU-R, STU-C or SRU.

3.1.15 span: The link between STU-C and STU-R, including regenerators.

3.1.16 spectral shaper: A device that reshapes the frequency characteristics of a signal.

3.1.17 stuff bits: Bits added to synchronize independent data streams.

3.1.18 synchronous: A clocking scheme in which the SHDSL frame and symbol clocks are based on the STU-C input transmit clock or a related network timing source.

3.1.19 **upstream**: STU-R to STU-C direction (remote terminal to central office).

3.2 Abbreviations

This Recommendation uses the following abbreviations:

α	The interface between the PMS-TC and TPS-TC layers in an STU-C
ß	The interface between the PMS-TC and TPS-TC layers in an STU-R
γ_C	The interface between the TPS-TC layer and the application specific section in an STU-C
γ_R	The interface between the TPS-TC layer and the application specific section in an STU-R
a_k	Convolutional Encoder Coefficients
AFE	Analogue Front End
AGC	Automatic Gain Control
b_k	Convolutional Encoder Coefficients
BER	Bit Error Ratio
bit/s	Bits per Second
C_k	The kth Precoder Coefficient
CLEI™	Common Language Equipment Identifier
CMRR	Common Mode Rejection Ratio
CO	Central Office
CPE	Customer Premises Equipment
CRC	Cyclic Redundancy Check
CRC-6	CRC of Order 6 (used in SHDSL frame)
crc(X)	CRC Check Polynomial
DAC	Digital-to-Analogue Converter
dBm	dB reference to 1 mW, i.e., 0 dBm = 1 mW
DC	Direct Current
DLL	Digital Local Line
DRR	Dynamic Rate Repartitioning
DS	Downstream
DSC	Dedicated Signalling Channel
DSL	Digital Subscriber Line
DUT	Device Under Test
EOC	Embedded Operations Channel
ES	Errored Second
f_s	Sampling rate
f_{sym}	Symbol rate
FCS	Frame Check Sequence

FEC	Forward Error Correction
FEXT	Far-End CrossTalk
FSW	Frame Synchronization Word
g(X)	Generating Polynomial for CRC
HDLC	High-level Data Link Control
HW	Hardware
I/F	Interface
kbit/s	Kilobits per second
LB	Longitudinal Balance
LCL	Longitudinal Conversion Loss
losd	Bit indicating Loss of signal at the application interface
LOSW	Loss Of Sync Word failure
LSB	Least Significant Bit
LT	Line Termination
m(X)	Message Polynomial for CRC
Mbit/s	Megabits per second
MSB	Most Significant Bit
MTU	Maintenance Termination Unit
NEXT	Near-End CrossTalk
NT	Network Termination
OAM	Operations, Administration and Maintenance
OH	Overhead
PAM	Pulse Amplitude Modulation
2-PAM	PAM having two levels (used at startup)
PBO	Power Back-Off
PL-OAM	Physical Layer – OAM
PMD	Physical Medium Dependent
PMMS	Power Measurement Modulation Session (Line Probe)
PMS-TC	Physical Medium-Specific TC Layer
ppm	Parts Per Million
PPP	Point-to-Point Protocol
ps	Power status bit
PSD	Power Spectral Density
PTD	Path Terminating Device (CO side terminating equipment)
PTM	Packet Transfer Mode
REG	Signal Regenerator
rms	Root mean square

RSP	Regenerator Silent Period bit
RX	Receiver
S/T	Logical interface between the STU-R and attached user terminal equipment
sb	stuff bit
sbid	stuff bit identified indicator bit
sega	segment anomaly indicator bit
segd	segment defect indicator bit
SES	Severely Errored Second
SHDSL	Single-Pair High-Speed DSL
SNR	Signal-to-Noise Ratio
SRU	SHDSL Regenerator Unit
STU	SHDSL Transceiver Unit
STU-C	STU at the Central Office
STU-R	STU at the Remote End
TBD	To Be Determined
TC	Transmission Convergence layer
TCM	Trellis Coded Modulation
TCM-ISDN	Time-Compression Multiplexed ISDN (specified in Appendix III/G.961 [B1])
TCPAM	Trellis Coded PAM (used in data mode)
TPS-TC	Transmission Protocol-Specific TC Layer
TX	Transmitter
U-C	Loop Interface – Central Office end
U-R	Loop Interface – Remote Terminal end
UAS	Unavailable Second
US	Upstream
UTC	Unable to Comply
V	Logical interface between STU-C and a digital network element such as one or more switching systems
xDSL	a collective term referring to any of the various types of DSL technologies

4 Reference models

4.1 STU-x functional model

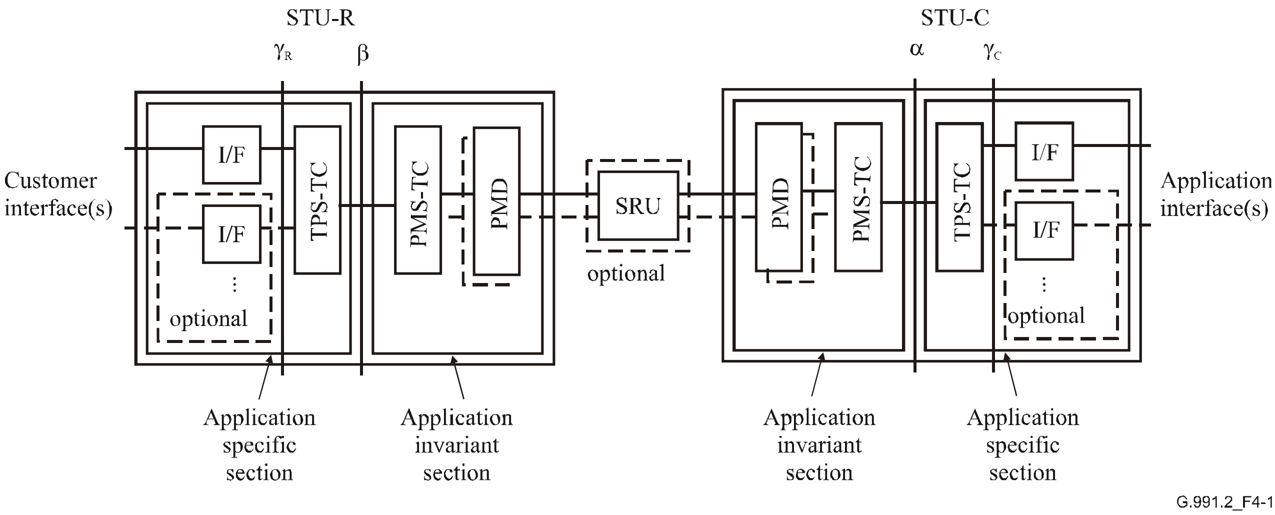


Figure 4-1/G.991.2 – STU-x functional model

Figure 4-1 is a block diagram of an SHDSL Transceiver Unit (STU) transmitter showing the functional blocks and interfaces that are referenced in this Recommendation. It illustrates the basic functionality of the STU-R and the STU-C. Each STU contains both an application invariant section and an application specific section. The application invariant section consists of the PMD and PMS-TC layers, while the application specific aspects are confined to the TPS-TC layer and device interfaces. As shown in the figure, one or more optional signal regenerators may also be included in an SHDSL span. Management functions, which are typically controlled by the operator's network management system, are not shown in the figure. See clause 9 for details on management. Remote power feeding, which is optionally provided across the span by the STU-C, is not illustrated in the figure.

The functions at the central office side constitute the STU-C (or Line Termination (LT)). The STU-C acts as the master both to the customer side functions of the STU-R (or Network Termination (NT)) and to any regenerators.

The STU-C and STU-R, along with the DLL (Digital Local Line) and any regenerators, make up an SHDSL span. The DLL may consist of a single copper twisted pair, or, in optional configurations, multiple copper twisted pairs. In the multi-pair cases, each STU contains multiple separate PMD layers, interfacing to a common PMS-TC layer. If enhanced transmission range is required, one or more signal regenerators may be inserted into the loop at intermediate points. These points shall be chosen to meet applicable criteria for insertion loss and loop transmission characteristics.

The principal functions of the PMD layer are:

- symbol timing generation and recovery;
- coding and decoding;
- modulation and demodulation;
- echo cancellation;
- line equalization;
- link startup.

The PMD layer functionality is described in detail in clause 6.

The PMS-TC layer contains the framing and frame synchronization functions, as well as the scrambler and descrambler. The PMS-TC layer is described in clause 7.

The PMS-TC is connected across the α and ß interfaces in the STU-C and the STU-R, respectively, to the TPS-TC layer. The TPS-TC is application specific and consists largely of the packaging of user data within the SHDSL frame. See clause 8 for details. This may include multiplexing, demultiplexing, and timing alignment of multiple user data channels. Supported TPS-TC user data framing formats are described in Annex E.

The TPS-TC layer communicates with the Interface blocks across the γ_R and γ_C interfaces. Depending upon the specific application, the TPS-TC layer may be required to support one or more channels of user data and associated interfaces. The definition of these interfaces is beyond the scope of this Recommendation.

Note that the α, ß, γ_R and γ_C interfaces are only intended as logical separations and need not be physically accessible.

4.2 User plane protocol reference model

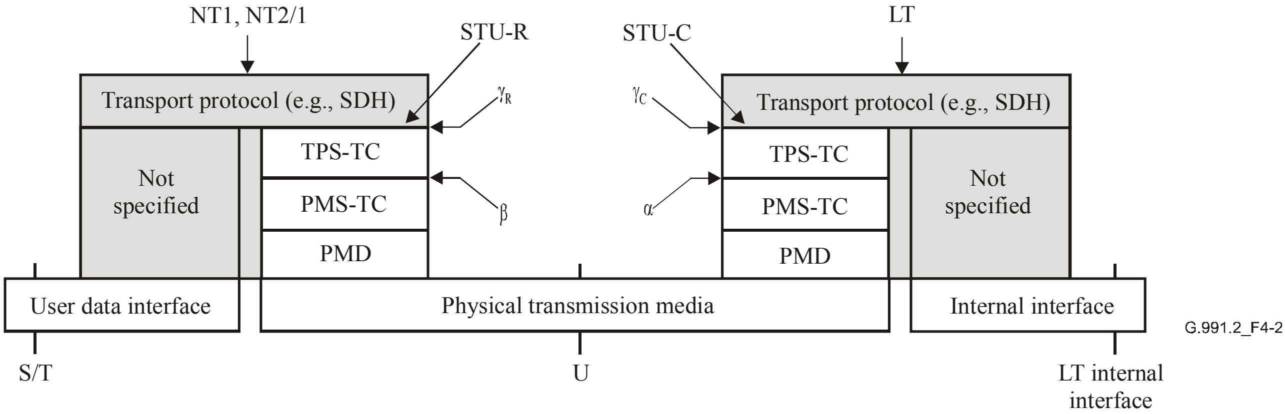


Figure 4-2/G.991.2 – User plane protocol reference model

The User Plane Protocol Reference Model, shown in Figure 4-2, is an alternate representation of the information shown in Figure 4-1. This figure is included to emphasize the layered nature of this Recommendation and to provide a view that is consistent with the generic xDSL models shown in ITU-T Rec. G.995.1 [B2].

4.3 Application models

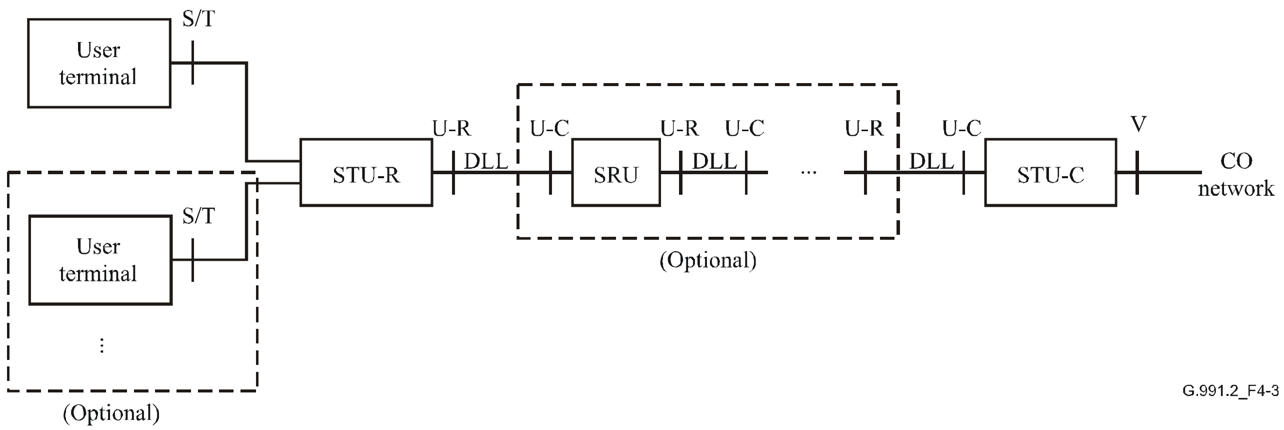


Figure 4-3/G.991.2 – Application model

Figure 4-3 is an application model for a typical SHDSL system, showing reference points and attached equipment. In such an application, an STU-R will typically connect to one or more user terminals, which may include data terminals, telecommunications equipment, or other devices. These connections to these pieces of terminal equipment are designated S/T reference points. The connection between STU-R and STU-C may optionally contain one or more SHDSL signal regenerators (SRUs). The connections to the DLLs that interconnect STUs and SRUs are designated U reference points. For each STU-x and SRU, the Network side connection is termed the U-R interface and the Customer side connection is termed the U-C interface. The STU-C typically connects to a Central Office network at the V reference point.

5 Transport capacity

This Recommendation specifies a two-wire operational mode for SHDSL transceivers that is capable of supporting user (payload) data rates from 192 kbit/s to 2.312 Mbit/s in increments of 8 kbit/s. The allowed rates are given by $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For $n = 36$, i is restricted to the values of 0 or 1. See Annexes A and B for details of specific regional requirements. Note that optional extensions described in Annex F allow user data rates up to 5696 bit/s.

This Recommendation also specifies an optional M-pair operational mode that is capable of supporting user (payload) data rates from $M \times 192$ kbit/s to $M \times 2.312$ Mbit/s in increments of $M \times 8$ kbit/s, where $1 \le M \le 4$. Note that optional extensions described in Annex F allow user data rates up to $M \times 5696$ kbit/s. Four-wire mode is identical to M-pair mode with M = 2, except for the method of assigning ordinal numbers to the wire pairs. In four-wire mode the ordinal numbers (the wire pair identification number) are assigned as described in 6.3, while in M-pair mode the ordinal numbers are assigned to wire pairs as described in 7.2.1.5. Again, see Annexes A and B for details of specific regional requirements and Annex F for extended data rates.

6 PMD layer functional characteristics

6.1 Data mode operation

6.1.1 STU data mode PMD reference model

A reference model of the data mode PMD layer of an STU-C or STU-R transmitter is shown in Figure 6-1.

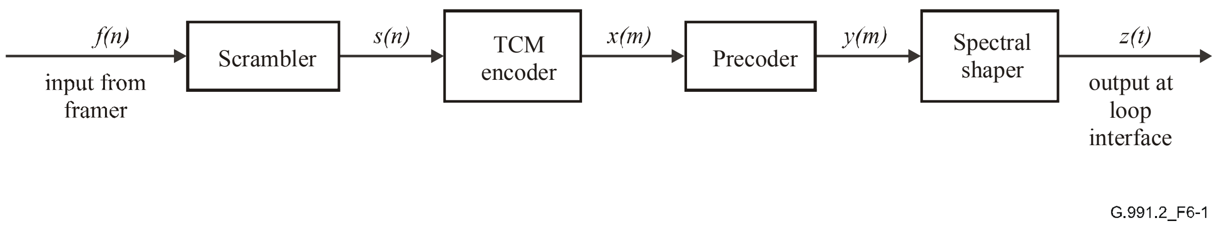


Figure 6-1/G.991.2 – Data mode PMD reference model

The time index n represents the bit time, the time index m represents the symbol time, and t represents analogue time. The input from the framer is $f(n)$, and $s(n)$ is the output of the scrambler. Both the framer and the scrambler are contained within the PMS-TC layer and are shown here for clarity. $x(m)$ is the output of the TCM (Trellis Coded Modulation) encoder, $y(m)$ is the output of the channel precoder, and $z(t)$ is the analogue output of the spectral shaper at the loop interface. When transferring K information bits per one-dimensional PAM symbol, the symbol duration is K times the bit duration, so the K values of n for a given value of m are $\{mK + 0, mK + 1, \dots, mK + K - 1\}$.

In the optional *M*-pair mode, *M* separate PMD sublayers are active – one for each wire pair. In this case, *n* represents the bit time for each wire pair rather than the aggregate system line rate.

6.1.1.1 PMD rates

The operation of the PMD layer at the specified information rate shall be as specified in A.5.1 or B.5.1. The operation of the PMD layer at the optional extended rates specified in Annex F shall be as specified in F.2.

6.1.2 TCM encoder

The block diagram of the TCM encoder is shown in Figure 6-2. The serial bit stream from the scrambler, *s(n)*, shall be converted to a *K*-bit parallel word at the *m*th symbol time, then processed by the convolutional encoder. The resulting $K + 1$-bit word shall be mapped to one of 2^{K+1} pre-determined levels forming *x(m)*.

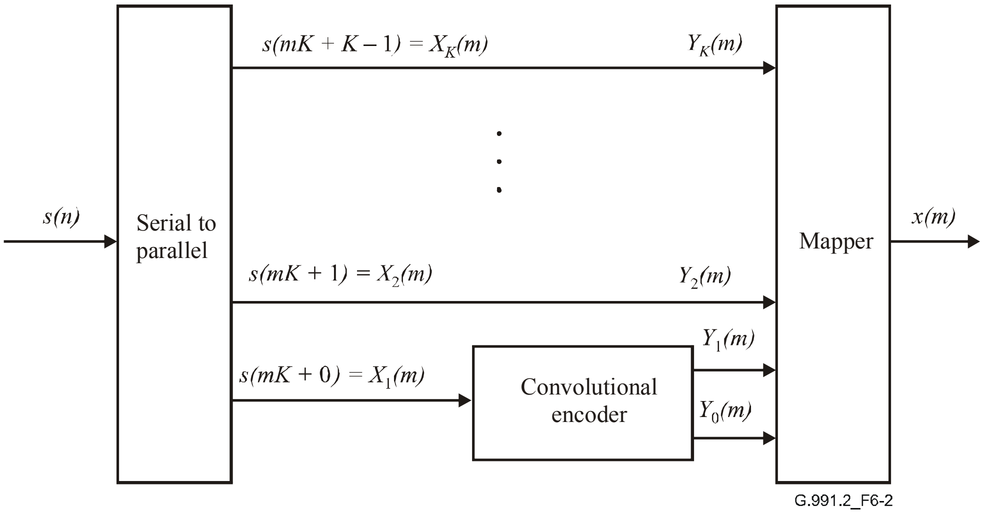


Figure 6-2/G.991.2 – Block diagram of the TCM encoder

6.1.2.1 Serial-to-parallel converter

The serial bit stream from the scrambler, *s(n),* shall be converted to a *K*-bit parallel word $\{X_1(m) = s(mK + 0), X_2(m) = s(mK + 1), \ldots , X_K(m) = s(mK + K - 1)\}$ at the *m*th symbol time, where $X_1(m)$ is the first input bit in time.

6.1.2.2 Convolutional encoder

Figure 6-3 shows the feedforward non-systematic convolutional encoder, where T_s is a delay of one symbol time, "⊕" is binary exclusive-OR, and "⊗" is binary AND. $X_1(m)$ shall be applied to the convolutional encoder, $Y_1(m)$ and $Y_0(m)$ shall be computed, then $X_1(m)$ shall be shifted into the shift register.

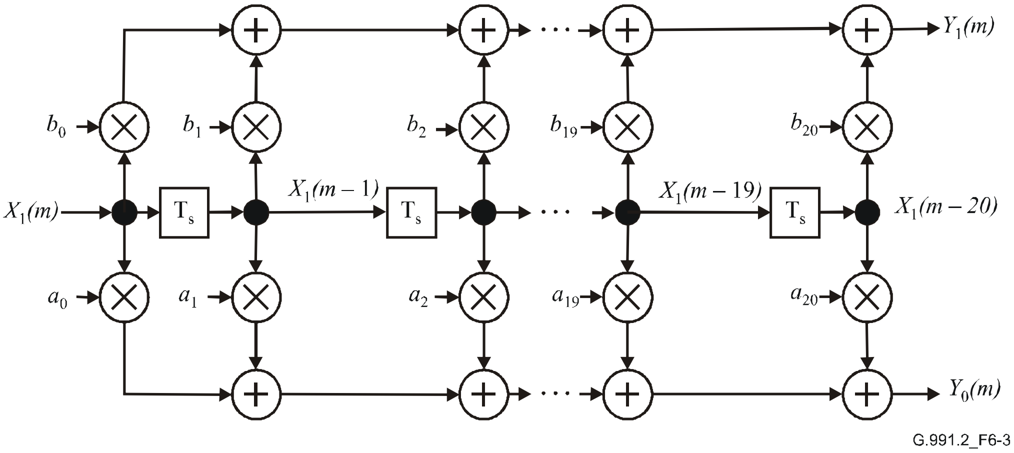


Figure 6-3/G.991.2 – Block diagram of the convolutional encoder

The binary coefficients a_i and b_i shall be passed to the encoder from the receiver during the activation phase specified in 7.2.1.3. A numerical representation of these coefficients is A and B where:

$$A = a_{20} \cdot 2^{20} + a_{19} \cdot 2^{19} + a_{18} \cdot 2^{18} + ... + a_0 \cdot 2^0\text{; and}$$

$$B = b_{20} \cdot 2^{20} + b_{19} \cdot 2^{19} + b_{18} \cdot 2^{18} + ... + b_0 \cdot 2^0$$

The choice of encoder coefficients is vendor specific. They shall be chosen such that the system performance requirements are satisfied (see Annex A and/or Annex B for performance requirements).

6.1.2.3 Mapper

The $K + 1$ bits $Y_K(m)$, ... , $Y_1(m)$, and $Y_0(m)$ shall be mapped to a level $x(m)$. Table 6-1 gives the bit to level mapping for 16-level mapping.

Table 6-1/G.991.2 – Mapping of bits to PAM levels

Y_3(m)	Y_2(m)	Y_1(m)	Y_0(m)	x(m) for 16-PAM
0	0	0	0	−15/16
0	0	0	1	−13/16
0	0	1	0	−11/16
0	0	1	1	−9/16
0	1	0	0	−7/16
0	1	0	1	−5/16
0	1	1	0	−3/16
0	1	1	1	−1/16
1	1	0	0	1/16
1	1	0	1	3/16
1	1	1	0	5/16
1	1	1	1	7/16
1	0	0	0	9/16
1	0	0	1	11/16
1	0	1	0	13/16
1	0	1	1	15/16

6.1.3 Channel precoder

The block diagram of channel precoder is shown in Figure 6-4, where T_s is a delay of one symbol time.

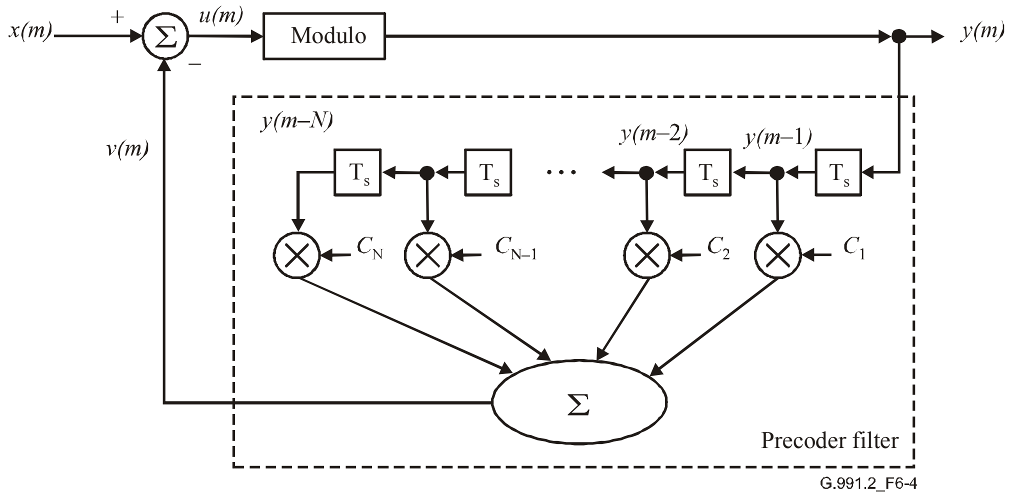


Figure 6-4/G.991.2 – Block diagram of the channel precoder

The coefficients of the precoder filter, C_k, shall be transferred to the channel precoder as described in 7.2.1.2. The output of the precoder filter, *v(m)*, shall be computed as follows:

$$v(m) = \sum_{k=1}^{N} C_k y(m-k)$$

Where $128 \leq N \leq 180$. The function of the modulo block shall be to determine *y(m)* as follows: for each value of *u(m)*, find an integer, *d(m)*, such that:

$$-1 \leq u(m) + 2d(m) < 1$$

and then

$$y(m) = u(m) + 2d(m)$$

6.1.4 Spectral shaper

The choice of spectral shape shall be region-specific. The details of PSDs for Regions A and B are given in A.4 and B.4. The details of PSDs for the optional extended rates in Annex F are given in F.4.

6.1.5 Power backoff

SHDSL devices shall implement Power Backoff, as specified in this clause. The selected power backoff value shall be communicated during pre-activation through the use of G.994.1 parameter selections.

The power backoff value shall be selected to meet the requirements shown in Table 6-2. The power backoff calculations are based on Estimated Power Loss (EPL), which is defined as:

Estimated Power Loss (dB) = TX Power (dBm) – Estimated RX Power (dBm),

evaluated for the data mode PSD.

No explicit specification is given herein for the method of calculating Estimated RX Power. Depending upon the application, this value may be determined based on line probe results, *a priori* knowledge, or G.994.1 tone levels.

The Power Backoff that is applied shall be no less than the Default Power Backoff, and it shall not exceed the Maximum Power Backoff Value.

Table 6-2/G.991.2 – Required power backoff values

Estimated power loss (dB)	Maximum power backoff (dB)	Default power backoff (dB)
EPL > 6	31	0
6 ≥ EPL > 5	31	1
5 ≥ EPL > 4	31	2
4 ≥ EPL > 3	31	3
3 ≥ EPL > 2	31	4
2 ≥ EPL > 1	31	5
1 ≥ EPL > 0	31	6

6.2 PMD activation sequence

This clause describes waveforms at the loop interface and associated procedures during activation mode. The direct specification of the performance of individual receiver elements is avoided when possible. Instead, the transmitter characteristics are specified on an individual basis and the receiver performance is specified on a general basis as the aggregate performance of all receiver elements. Exceptions are made for cases where the performance of an individual receiver element is crucial to interoperability. In 6.2.2, "convergence" refers to the state where all adaptive elements have reached steady-state. The declaration of convergence by a transceiver is therefore vendor dependent. Nevertheless, actions based on the state of convergence are specified to improve interoperability.

6.2.1 PMD activation reference model

The reference model of the activation mode of an STU-C or STU-R transmitter is shown in Figure 6-5.

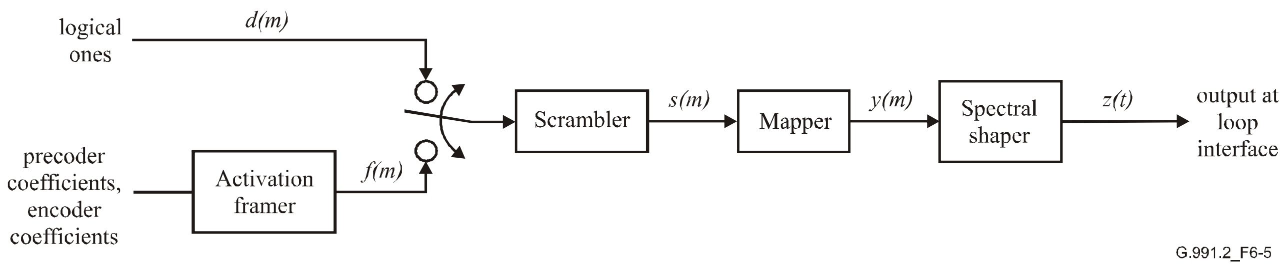


Figure 6-5/G.991.2 – Activation reference model

The time index *m* represents the symbol time, and *t* represents analogue time. Startup uses 2-PAM modulation, so the bit time is equivalent to the symbol time. The output of the activation framer is *f(m)*, the framed information bits. The output of the scrambler is *s(m)*. Both the framer and the scrambler are contained within the PMS-TC layer and are shown here only for clarity. The output of the mapper is *y(m)*, and the output of the spectral shaper at the loop interface is *z(t)*. *d(m)* is an initialization signal that shall be logical ones for all *m*. The modulation format shall be uncoded 2-PAM, at the symbol rate selected for data mode operation.

In devices supporting the optional *M*-pair mode, the core activation procedure shall be considered as an independent procedure for each pair. Such devices shall be capable of detecting the completion of activation for all pairs and upon completion shall initiate the transmission of user data over all pairs.

6.2.2 PMD activation sequence description

The timing diagram for the activation sequence is given in Figure 6-6. The state transition diagram for the startup sequence is given in Figure 6-7. Each signal in the activation sequence shall satisfy the tolerance values listed in Table 6-3.

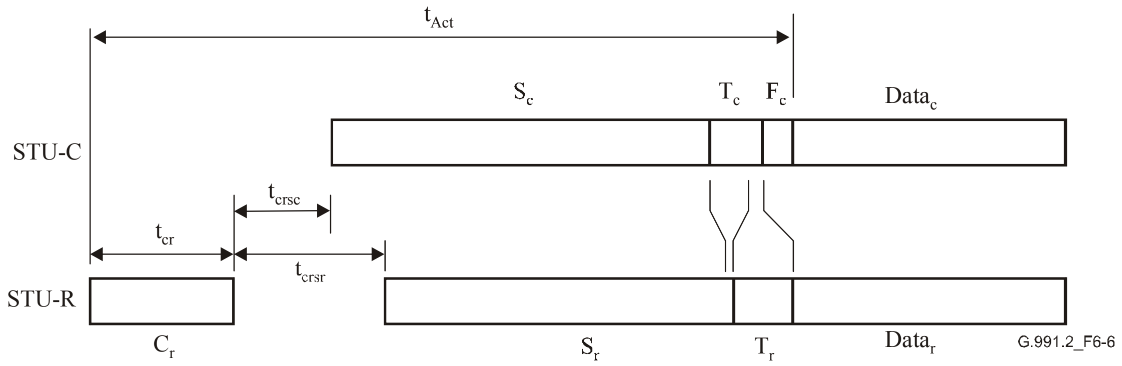


Figure 6-6/G.991.2 – Timing diagram for activation sequence

Figure 6-6a shows the total activation sequence at a high level for G.991.2, which includes pre-activation and core activation. Included as an example in the pre-activation phase are two sessions of handshake per ITU-T Rec. G.994.1 and line probe.

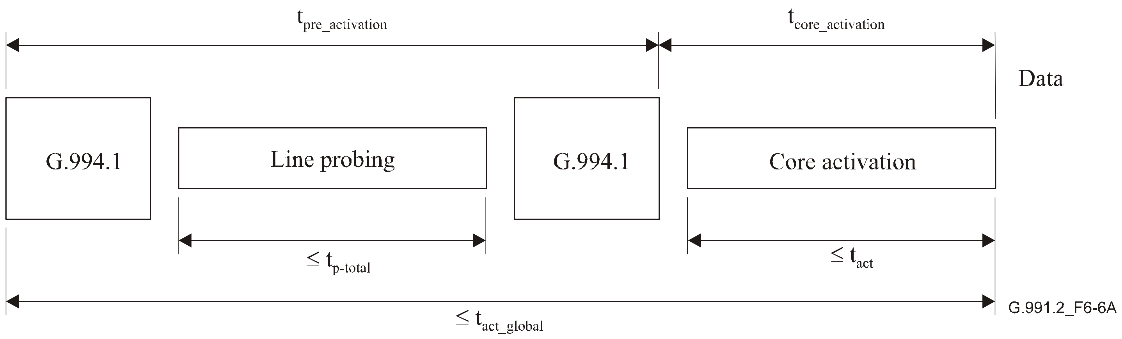


Figure 6-6a/G.991.2 – G.991.2 total activation sequence

The global activation time is the sum of the pre-activation and core activation times. Therefore, from Figure 6-6a,

$$t_{pre\_activation} + t_{core\_activation} \leq t_{act\_global}$$

where $t_{pre\_activation}$ is the combined duration of the G.994.1 sessions (see 6.4) and line probing (see 6.3), $t_{core\_activation}$ is the core activation duration (see 6.2). The values for t_{act} and t_{act_global} are defined in Table 6-3. The value for $t_{p\text{-}total}$ is given in Table 6-5.

Table 6-3/G.991.2 – Timing for activation signals

Time	Parameter	Reference	Nominal value	Tolerance
t_{cr}	Duration of C_r	6.2.2.1	$1 \times \beta$ s[a)]	±20 ms
t_{crsc}	Time from end of C_r to beginning of S_c	6.2.2.2	500 ms	±20 ms
t_{crsr}	Time from end of C_r to beginning of S_r	6.2.2.3	$1.5 \times \beta$ s[a)]	±20 ms
t_{act}	Maximum time from start of C_r to $Data_r$		$15 \times \beta$ s[a)]	
$t_{payloadValid}$	Maximum time from start of $Data_c$ or $Data_r$ to valid SHDSL payload data		1 s	
$t_{silence}$	Minimum silence time from exception		2 s	

Table 6-3/G.991.2 – Timing for activation signals

Time	Parameter	Reference	Nominal value	Tolerance
	condition to start of train			
t_{PLL}	Maximum time from start of S_c to STU-R PLL lock		5 s	
t_{act_global}	Time from start of initial pre-activation session (6.3) to $Data_r$ [b)]		30 s	
a) β is dependent on bit rate. β = 1 for n > 12, β = 2 for n ≤ 12, where n is defined in clause 5. b) In the majority of the cases, t_{act_global} will be less than 30 seconds. However, since the definition of the handshake mechanism in ITU-T Rec. G.994.1 is outside the scope of this Recommendation, a maximum value t_{act_global} cannot be assured.				

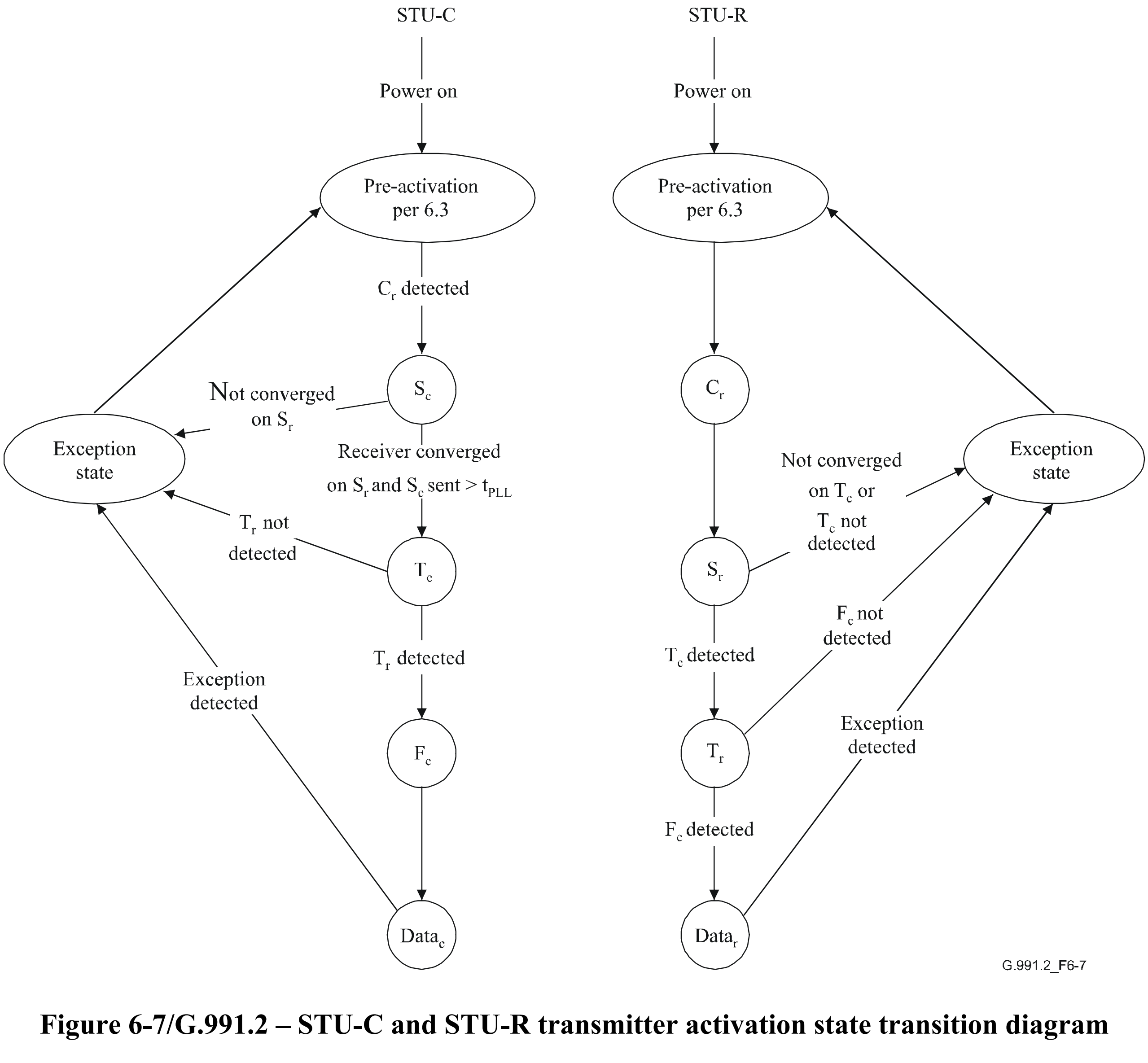


Figure 6-7/G.991.2 – STU-C and STU-R transmitter activation state transition diagram

6.2.2.1 Signal C_r

After exiting the pre-activation sequence (per ITU-T Rec. G.994.1 [2], see 6.3 for details), the STU-R shall send C_r. Waveform C_r shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for C_r shall be the upstream PSD mask, as negotiated during pre-activation sequence. C_r shall have a duration of t_{cr} and shall be sent 0.3 s after the end of pre-activation.

NOTE – The end of pre-activation can be defined in two ways according to ITU-T Rec. G.994.1. For the purpose of this Recommendation, the end of pre-activation will be from the end of the ACK(1) message transmission plus the required timers. The minimum and maximum values of those timers are 0.04 and 1.0 second. Therefore, the total time between the end of the ACK(1) message and the beginning of C_r should be between 0.34 and 1.3 seconds.

6.2.2.2 Signal S_c

After detecting C_r, the STU-C shall send S_c. Waveform S_c shall be generated by connecting the signal *d(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for S_c shall be the downstream PSD mask, as negotiated during pre-activation sequence. S_c shall be sent t_{crsc} after the end of C_r. If the STU-C does not converge while S_c is transmitted, it shall enter the exception state (6.2.2.8).

6.2.2.3 Signal S_r

The STU-R shall send S_r, beginning t_{crsr} after the end of C_r. Waveform S_r shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for S_r shall be the same as for C_r. If the STU-R does not converge and detect T_c while S_r is transmitted, it shall enter the exception state (6.2.2.8). The method used to detect T_c is vendor dependent. In timing modes supporting loop timing, waveform S_r and all subsequent signals transmitted from the STU-R shall be loop timed, i.e., the STU-R symbol clock shall be locked to the STU-C symbol clock.

6.2.2.4 Signal T_c

Once the STU-C has converged and has been sending S_c for at least t_{PLL} (Table 6-3), it shall send T_c. Waveform T_c contains the precoder coefficients and other system information. T_c shall be generated by connecting the signal *f(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for T_c shall be the same as for S_c. The signal *f(m)* is the activation frame information as described in 7.2.1. If the STU-C does not detect T_r while sending T_c, it shall enter the exception state (6.2.2.8). The method used to detect T_r is vendor dependent.

6.2.2.5 Signal T_r

Once the STU-R has converged and has detected the T_c signal, it shall send T_r. Waveform T_r contains the precoder coefficients and other system information. T_r shall be generated by connecting the signal *f(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for T_r shall be the same as for C_r. The signal *f(m)* is the activation frame information as described in 7.2.1. If the STU-R does not detect F_c while sending T_r, it shall enter the exception state (6.2.2.8). The method used to detect F_c is vendor dependent.

6.2.2.6 Signal F_c

Once the STU-C has detected T_r and completed sending the current T_c frame, then it shall send F_c. The first bit of the first F_c frame shall follow contiguously the last bit of the last T_c frame. Signal F_c shall be generated by connecting the signal *f(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for F_c shall be the same as for S_c. The signal *f(m)* is the activation frame information as described in 7.2.1 with the following exceptions: the frame sync word shall be reversed in time, and the payload information bits shall be set to arbitrary values. The CRC shall be calculated on this arbitrary-valued payload. The signal F_c shall be transmitted for exactly two activation frames. As soon as the first bit of F_c is transmitted, the payload data in the T_r signal shall be ignored.

6.2.2.7 $Data_c$ and $Data_r$

Within 200 symbols after the end of the second frame of F_c, the STU-C shall enter data mode and send $Data_c$, and the STU-R shall enter data mode and send $Data_r$. These TCPAM signals are described in 6.1. The PSD mask for $Data_r$ and for $Data_c$ shall be according to A.4 or B.4, as negotiated during the pre-activation sequence. There is no required relationship between the end of the activation frame and any bit within the SHDSL data-mode frame. $t_{payloadValid}$ (Table 6-3) after the end of F_c, the SHDSL payload data shall be valid at the α or ß interface.

6.2.2.8 Exception state

If activation is not achieved within t_{act} (Table 6-3) or if any exception condition occurs, then the exception state shall be invoked. During the exception state the STU shall be silent for at least $t_{silence}$ (Table 6-3), then wait for transmission from the far end to cease, then return to the corresponding initial startup state; the STU-R and STU-C shall begin pre-activation, as per 6.3.

6.2.2.9 Exception condition

An exception condition shall be declared during activation if any of the timeouts in Table 6-3 expire or if any vendor-defined abnormal event occurs. An exception condition shall be declared during data mode if a vendor-defined abnormal event occurs. A vendor-defined abnormal event shall be defined as any event that requires a loop restart for recovery.

6.2.3 Framer and scrambler

The activation mode framer and scrambler are described in 7.2.

6.2.4 Mapper

The output bits from the scrambler, *s(m)*, shall be mapped to the output level, *y(m)*, as follows:

Table 6-4/G.991.2 – Bit-to-level mapping

Scrambler output *s(m)*	Mapper output level, *y(m)*	Data mode index
0	–9/16	0011
1	+9/16	1000

These levels, corresponding to the scrambler outputs 0 and 1, shall be identical to the levels in the 16-TCPAM constellation (Table 6-1) corresponding to indexes 0011 and 1000, respectively.

6.2.5 Spectral shaper

The same spectral shaper shall be used for data mode and activation mode as described in A.4 or B.4. For the optional extended rates in Annex F, the same spectral shaper shall be used for data mode and activation mode as described in F.4.

6.2.6 Timeouts

Table 6-3 shows the system timeouts and their values. t_{act} shall be the maximum time from the start of C_r to the start of $Data_r$. It controls the overall time of the train. $t_{payloadValid}$ is the time between the start of data mode and the instant at which the SHDSL payload data is valid (this accounts for settling time, data flushing, frame synchronization, etc). $t_{silence}$ shall be the minimum time in the exception state in which the STU-C or STU-R is silent before returning to pre-activation (per ITU-T Rec. G.994.1 [2], see 6.3 for details). t_{PLL} shall be the time allocated for the STU-R to pull in the STU-C timing. The STU-C shall transmit S_c for at least t_{PLL}.

6.3 PMD pre-activation sequence

This clause describes waveforms at the loop interface and associated procedures during pre-activation mode. The direct specification of the performance of individual receiver elements is avoided when possible. Instead, the transmitter characteristics are specified on an individual basis and the receiver performance is specified on a general basis as the aggregate performance of all receiver elements. Exceptions are made for cases where the performance of an individual receiver element is crucial to interoperability.

In the optional 4-wire mode, Pair 1 and Pair 2 shall be determined during the pre-activation sequence per the procedures defined in Annex B/G.994.1 entitled, "Operation over multiple wire pairs". Pair 1 shall be defined as the pair on which the final G.994.1 transaction is conducted.

Four-wire mode is identical to *M*-pair mode with $M = 2$, except for the method of assigning ordinal numbers to the wire pairs. In the optional *M*-pair mode, the ordering of wire pairs shall be determined as per 7.2.1.5.

6.3.1 PMD pre-activation reference model

The reference model of the pre-activation mode of an STU-C or STU-R transmitter is shown in Figure 6-8.

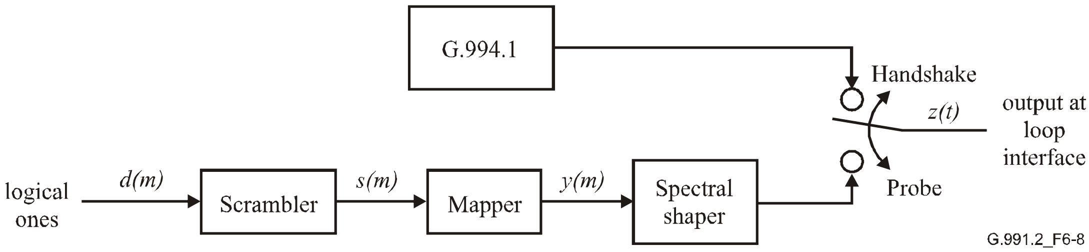


Figure 6-8/G.991.2 – Pre-activation reference model

The time index *m* represents the symbol time, and *t* represents analogue time. Since the probe signal uses 2-PAM modulation, the bit time is equivalent to the symbol time. The output of the scrambler is *s(m)*. The scrambler used in the PMD pre-activation may differ from the PMS-TC scrambler used in activation and data modes. See 6.3.3 for details of the pre-activation scrambler. The output of the mapper is *y(m)*, and the output of the spectral shaper at the loop interface is *z(t)*. *d(m)* is an initialization signal that shall be logical ones for all *m*. The probe modulation format shall be uncoded 2-PAM, with the symbol rate, spectral shape, duration and power backoff selected by ITU-T Rec. G.994.1. Probe results shall be exchanged by ITU-T Rec. G.994.1.

In the optional *M*-pair mode, the G.994.1 exchange shall follow the defined procedures for multi-pair operation. In this case, Signals P_{ri} and P_{ci}, as described below, shall be sent in parallel on all wire pairs.

6.3.2 PMD pre-activation sequence description

A typical timing diagram for the pre-activation sequence is given in Figure 6-9. Each signal in the pre-activation sequence shall satisfy the tolerance values listed in Table 6-5.

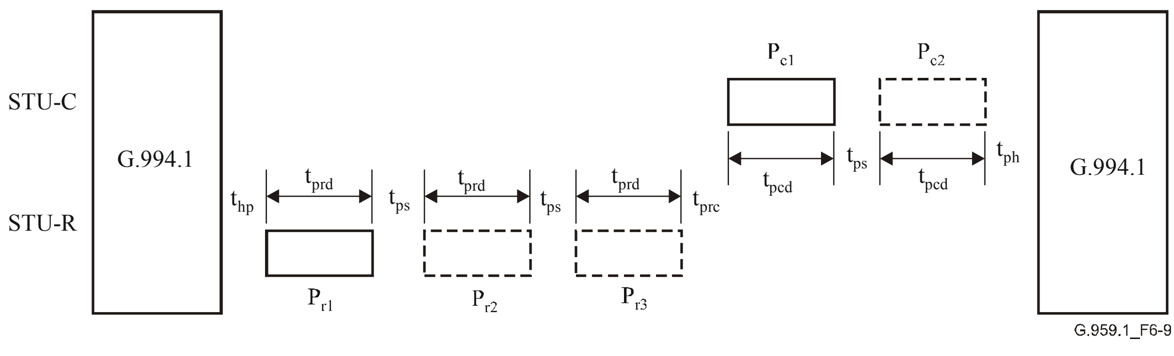


Figure 6-9/G.991.2 – Typical timing diagram for pre-activation sequence

Table 6-5/G.991.2 – Timing for pre-activation signals (Note)

Time	Parameter	Nominal value	Tolerance
t_{hp}	Time from end of handshake to start of remote probe	0.2 s	±10 ms
t_{prd}	Duration of remote probe	Selectable from 50 ms to 3.1 s	±10 ms
t_{ps}	Time separating two probe sequences	0.2 s	±10 ms
t_{prc}	Time separating last remote and first central probe sequences	0.2 s	±10 ms
t_{pcd}	Duration of central probe	Selectable from 50 ms to 3.1 s	±10 ms
t_{ph}	Time from end of central probe to start of handshake	0.2 s	±10 ms
$t_{p\text{-}total}$	Total probe duration, from end of the first G.994.1 session to the start of the second G.994.1 session	10 s maximum	
NOTE – Tolerances are relative to the nominal or ideal value. They are not cumulative across the pre-activation sequence.			

6.3.2.1 Signal P_{ri}

If the optional line probe is selected during the G.994.1 session (see ITU-T Rec. G.994.1 [2] for details), the STU-R shall send the remote probe signal. The symbol rate for the remote probe signal shall be negotiated during the G.994.1 session, and shall correspond to the symbol rate used during activation for the specified data rate. If multiple remote probe symbol rates are negotiated during the G.994.1 session, then multiple probe signals will be generated, starting with the lowest symbol rate negotiated and ending with the highest symbol rate negotiated. If both symmetric and asymmetric PSD probe signals are selected, the symmetric PSD probe signals shall be sent first, in order of ascending symbol rate, followed by the asymmetric PSD probe signals in order of ascending symbol rate. If symmetric PSD probe signals are selected from both Annexes A and F, then the symmetric PSD probe signals from Annex A will be sent first, followed by the symmetric PSD probe signals from Annex F, all in order of ascending symbol rate. If "transmit silence" is negotiated, then a probe signal consisting of transmitted silence will precede all other probe signals. P_{ri} is the ith probe signal (corresponding to the ith symbol rate negotiated or silence). Waveform P_{ri} shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in Figure 6-8. The PSD mask for P_{ri} shall be the upstream PSD mask used for signal C_r at the same symbol rate, and shall be selectable between the PSDs for activating at data rates of 192 kbit/s to 2304 kbit/s in steps of 64 kbit/s. Note that optional extensions described in Annex F allow the selection of P_{ri} masks corresponding to data rates up to 5696 kbit/s. Alternatively, waveform P_{ri} can be selected to transmit silence. The duration (t_{prd}) and power backoff shall be the same for all P_{ri}, and shall be negotiated during the G.994.1 session. The duration shall be selectable between 50 ms and 3.1 s in steps of 50 ms, and the power backoff shall be selectable between 0 dB and 15 dB in steps of 1 dB. The probe signal power backoff can be selected using either the received G.994.1 signal power or *a priori* knowledge. If no information is available, implementors are encouraged to select a probe power backoff of at least 6 dB. The first remote probe signal shall begin t_{hp} after the end of the G.994.1 session. There shall be a t_{ps} second silent interval between successive remote probe signals.

In the optional *M*-pair mode, P_{ri} shall be sent in parallel on all wire pairs.

6.3.2.2 Signal P_{ci}

The STU-C shall send the central probe signal t_{prc} after the end of the last remote probe signal. The symbol rate for the central probe signal shall be negotiated during the G.994.1 session, and shall correspond to the symbol rate used during activation for the specified data rate. If multiple central probe symbol rates are negotiated during the G.994.1 session, then multiple probe signals will be generated, starting with the lowest symbol rate negotiated and ending with the highest symbol rate negotiated. If both symmetric and asymmetric PSD probe signals are selected, the symmetric PSD probe signals shall be sent first, in order of ascending symbol rate, followed by the asymmetric PSD probe signals in order of ascending symbol rate. If symmetric PSD probe signals are selected from both Annexes A and F, then the symmetric PSD probe signals from Annex A will be sent first, followed by the symmetric PSD probe signals from Annex F, all in order of ascending symbol rate. If "transmit silence" is negotiated, then a probe signal consisting of transmitted silence will precede all other probe signals. P_{ci} is the ith probe signal (corresponding to the ith symbol rate negotiated or silence). Waveform P_{ci} shall be generated by connecting the signal *d(m)* to the input of the STU-C scrambler as shown in Figure 6-8. The PSD mask for P_{ci} shall be the downstream PSD mask used for signal S_c at the same symbol rate, and shall be selectable between the PSDs for activating at data rates of 192 kbit/s to 2304 kbit/s in steps of 64 kbit/s. Note that optional extensions described in Annex F allow the selection of P_{ci} masks corresponding to data rates up to 5696 kbit/s. Alternatively, waveform P_{ci} can be selected to transmit silence. The duration (t_{pcd}) and power backoff shall be the same for all P_{ci}, and shall be negotiated during the G.994.1 session. The duration shall be selectable between 50 ms and 3.1 s in steps of 50 ms, and the power backoff shall be selectable between 0 dB and 15 dB in steps of 1 dB. The probe signal power backoff can be selected using either the received G.994.1 signal power or *a priori* knowledge. If no information is available, implementors are encouraged to select a probe power backoff of at least 6 dB. There shall be a t_{ps} silent interval between successive central probe signals, and there shall be a t_{ph} second silent interval between the last central probe signal and the start of the following G.994.1 session.

In the optional *M*-pair mode, P_{ci} shall be sent in parallel on all wire pairs.

6.3.3 Scrambler

The pre-activation mode scrambler shall have the same basic structure as the data mode scrambler, but may employ a different scrambler polynomial. During the G.994.1 session, the scrambler polynomial for the line probe sequence shall be selected by the receiver from the set of allowed scrambler polynomials listed in Table 6-6. The transmitter shall support all the polynomials in Table 6-6. During the line probe sequence, the transmit scrambler shall use the scrambler polynomial selected by the receiver during the G.994.1 session. The scrambler shall be initialized to all zeros.

Table 6-6/G.991.2 – Pre-activation scrambler polynomials

Polynomial index (i_2, i_1, i_0)	STU-C polynomial	STU-R polynomial
0 0 0	$s(m) = s(m-5) \oplus s(m-23) \oplus d(m)$	$s(m) = s(m-18) \oplus s(m-23) \oplus d(m)$
0 0 1	$s(m) = s(m-1) \oplus d(m)$	$s(m) = s(m-1) \oplus d(m)$
0 1 0	$s(m) = s(m-2) \oplus s(m-5) \oplus d(m)$	$s(m) = s(m-3) \oplus s(m-5) \oplus d(m)$
0 1 1	$s(m) = s(m-1) \oplus s(m-6) \oplus d(m)$	$s(m) = s(m-5) \oplus s(m-6) \oplus d(m)$
1 0 0	$s(m) = s(m-3) \oplus s(m-7) \oplus d(m)$	$s(m) = s(m-4) \oplus s(m-7) \oplus d(m)$
1 0 1	$s(m) = s(m-2) \oplus s(m-3) \oplus s(m-4) \oplus s(m-8) \oplus d(m)$	$s(m) = s(m-4) \oplus s(m-5) \oplus s(m-6) \oplus s(m-8) \oplus d(m)$
1 1 0	Reserved	Reserved
1 1 1	Not Allowed	Not Allowed

6.3.4 Mapper

The output bits from the scrambler, *s(m)*, shall be mapped to the output level, *y(m)*, as described in 6.2.4.

6.3.5 Spectral shaper

The same spectral shaper shall be used for data mode and activation mode as described in 6.1.4.

6.3.6 PMMS target margin

PMMS target margin is used by the receiver to determine if a data rate can be supported with this margin under current noise and/or reference worst-case noise specified in Annexes A and B. A data rate may be included in the capabilities list resulting from line probe only if the estimated SNR associated with that data rate minus the SNR required for BER = 10^{-7} is greater than or equal to target margin in dB. If both worst-case target margin and current-condition target margin are specified, then the capabilities exchanged shall be the intersection of data rates calculated using each noise condition separately.

The use of negative target margins with respect to reference worst-case noise corresponds to reference noise with fewer disturbers. This may be applicable when the number of disturbers is known to be substantially fewer than specified by the reference worst-case noise. Use of negative target margins with respect to current-conditions is not advised. Use of the current-condition target margin mode may result in retrains if the noise environment changes significantly.

The negotiation of the target margins is done as follows:

The target margins to be used by both the STU-C and the STU-R for determining the supported data rates are under the control of the STU-C. In the PMMS parameter exchange, the STU-C shall set the upstream and downstream PMMS target margins to identical values. This does not imply that the worst-case and current-conditions target margins are the same.

To determine which data rates the STU-C can support, the STU-C can choose to use the upstream PMMS target margin transmitted by the STU-R in the PMMS parameter exchange, or the STU-C may choose to use an alternative internal value for the PMMS target margins. The STU-R shall use the downstream PMMS target margin parameters sent by the STU-C for determining which data rates the STU-R can support.

This procedure is applicable to both the current-condition and the worst-case target margins.

6.4 G.994.1 pre-activation sequence

As noted in 6.3, ITU-T Rec. G.994.1 [2] shall be used to begin the pre-activation sequence. A second G.994.1 sequence shall follow the pre-activation line probe, as described in that clause. The G.994.1 protocol shall be the mechanism for exchanging capabilities and negotiating the operational parameters for each SHDSL connection. The use of a line probe sequence, as described in 6.3, is optional. If each STU has sufficient *a priori* knowledge of the line characteristics and the capabilities of the other STU, either from a previous connection or from user programming, the line probe sequence may be bypassed. In this case, the G.994.1 sequence will be followed by SHDSL activation, as described in 6.2.

6.4.1 G.994.1 code point definitions

The following definitions shall be applied to the SHDSL parameters specified in ITU-T Rec. G.994.1:

6.4.1.1 base data rate/PSD: These octets are used as follows:

– for PMMS, they indicate rates for line probing segments;

– for training, they indicate payload data rates;

Separate bits are provided for symmetric and asymmetric PSDs.

NOTE – In CLR, upstream training parameters indicate what data mode rates the STU-R is capable of transmitting, and downstream training parameters indicate what data mode rates the STU-R is capable of receiving. In CL, downstream training parameters indicate what data mode rates the STU-C is capable of transmitting, and upstream training parameters indicate what data mode rates the STU-C is capable of receiving. If optional line probe is used, the receiver training parameters will be further limited by the probe results. If repeaters are used, the training parameters of the SRU-R will be further limited by the training parameters of all downstream SRUs and the STU-R.

6.4.1.2 clock modes: Set to indicate clock mode, as defined in Table 10-1.

6.4.1.3 diagnostic mode: Set to indicate a diagnostic mode train (for use with SRUs).

6.4.1.4 DRR support: Indicates whether DRR is supported. See E.10.3.

6.4.1.5 four-wire: Set to indicate four-wire operation.

6.4.1.6 lead time: Indicates the lead time of DRR protocol responses, measured as a number of SHDSL frames. The range of supported values is from 1 to 15. See E.10.3.5.

6.4.1.7 low latency: Set to indicate that low latency operation, as defined in 11.5, is required. If not set, an STU may choose a higher latency encoding scheme.

6.4.1.8 *M*-pair count: Indicates the number of pairs used in the optional *M*-pair mode.

6.4.1.9 multiple-pair operation: Set to indicate *M*-pair mode. Four-wire mode is identical to *M*-pair mode with M = 2, except for the method of assigning ordinal numbers to the wire pairs. In four-wire mode, the ordinal numbers (i.e., the wire pair identification number) are assigned as described in 6.3; while in *M*-pair mode, the ordinal numbers are assigned to wire pairs as described in 7.2.1.5.

6.4.1.10 PBO: Power Backoff (in 1.0 dB increments).

6.4.1.11 PMMS duration: The length of each line probe (PMMS) segment (in 50 ms increments).

6.4.1.12 PMMS mode: An indication that an STU (or SRU) is prepared to begin a PMMS ("Power Measurement Modulation Session", or Line Probe) using the associated parameters.

6.4.1.13 PMMS scrambler: The scrambler polynomial used during line probe (PMMS). See 6.3.3.

6.4.1.14 PMMS target margin: If worst-case target margin is selected, target margin is relative to reference worst-case crosstalk specified in Tables A.13 and B.14. If current-condition target margin is selected, specified target margin is relative to noise measured during line probe. The 5-bit target margin is specified by (bits 5-1 × 1.0 dB) – 10 dB. For example, 101111_2 in the worst-case PMMS target margin octet corresponds to 15 dB – 10 dB = 5 dB target margin relative to reference worst-case noise.

If the capability for PMMS mode is indicated in a G.994.1 CLR/CL capabilities exchange, both target margin octets shall be sent. The specific values for target margin shall be ignored during the capabilities exchange, as all STUs (and SRUs) shall be capable of evaluating the results of PMMS using both types of target margin.

6.4.1.15 Regenerator Silent Period (RSP): A bit used to force an STU or SRU into a 1-minute silent interval to facilitate startup of spans including regenerators.

6.4.1.16 SRU: Set to indicate that the unit is a Signal Regenerator and not an STU.

6.4.1.17 stuff bits: Indicates the value that the upstream and downstream *stb*1 – *stb*4 bits shall take on. See 7.1.2.7 for details.

6.4.1.18 sub-data rate: For symmetric PSDs, the data rate octets indicate the base data rate in 64 kbit/s increments ($n \times 64$ kbit/s). The sub-data rate bits indicate additional 8 kbit/s increments ($i \times 8$ kbit/s) of data. The total payload data rate is set by: base data rate + sub-data rate. The sub-data rate bits do not apply to the asymmetric 2.048 Mbit/s, and 2.304 Mbit/s PSDs (from Annex B). For the asymmetric 768 or 776 kbit/s and asymmetric 1.536 or 1.544 Mbit/s PSDs (from Annex A), the base data rate bits indicate 768 kbit/s or 1.536 Mbit/s, and the sub-data rate bits for 0 and 8 kbit/s are valid for selecting the total payload data rate.

6.4.1.19 sync word: Indicates the value that the upstream and downstream $sw1 - sw14$ bits shall take on. See 7.1.2.1 for details.

6.4.1.20 TPS-TC: The TPS-TC mode is selected from the set of modes specified in Annex E.

6.4.1.21 training mode: An indication that an STU (or SRU) is prepared to begin SHDSL activation using the associated parameters.

6.4.1.22 warm-start enable: Set to indicate that warm-start is available. See Annex H.

6.4.2 G.994.1 tone support

SHDSL devices shall support half-duplex mode G.994.1 operation using the A4 carrier set from the 4 kHz signalling family. Manufacturers are encouraged to support additional carrier sets, the 4.3125 kHz signalling family, and full-duplex operation of G.994.1 to provide interoperable handshake sequences with other types of DSL equipment.

6.4.3 G.994.1 transactions

If no *a priori* capabilities information is available to the STU-R, it should begin the G.994.1 session by initiating Transaction C (CLR/CL). Otherwise, it may begin immediately with one of the mode selection transactions (e.g., A or B). In this capabilities exchange (CLR/CL sequence), each unit shall indicate the functions that it is currently capable of performing. This means that user options that have been disabled shall not be indicated as capabilities of the unit. If a unit's capabilities change due to user option settings or other causes, that unit shall cause a capabilities exchange to occur during the next G.994.1 session.

If both the STU-R and STU-C indicate the capability for line probing and no *a priori* information exists concerning the characteristics of the loop, the STU-R should initiate Transaction D (MP/MS/Ack(1)) by sending an MP with the G.991.2 line probe mode selected. This MP message shall include parameters for the downstream line probe sequence. The STU-C shall then issue a corresponding MS message containing the upstream line probe parameters and an echo of the downstream line probe parameters. Following an Ack(1) from the STU-R, the units shall exit G.994.1 and enter the G.991.2 line probe mode, as described in 6.3. Following the completion of line probing, the STU-C shall initiate a new G.994.1 session. The STU-R shall then initiate a Transaction C (CLR/CL) capabilities exchange to indicate the results of the line probe. Each unit shall, in this exchange, indicate the intersection of its capabilities and the capabilities of the loop, as determined during the line probe sequence. The PBO octet shall be used to indicate the desired received Power Backoff. Following this second capabilities exchange, the units may use any valid transaction to select operational SHDSL parameters.

Following the selection of the G.991.2 parameter set, G.994.1 shall terminate and the SHDSL activation sequence (6.2) shall begin.

6.4.4 Operation with signal regenerators

In general, SRUs will act as STUs during G.994.1, as described in 6.4.3. In some situations, however, they are required to issue "Regenerator Silent Period" (via the G.994.1 RSP bit) mode selections rather than selecting a G.991.2 operational mode, as described in Annex D and Appendix II. The parameters that SRUs report during capabilities exchanges are also slightly different. The advertised capabilities of an SRU-R shall be the intersection of its own capabilities and those reported across the regenerator's internal interface as indicative of the capabilities of the downstream units and line segments. The lone exception to this rule shall be the PBO octet, which shall be considered as a local parameter for each segment.

7 PMS-TC layer functional characteristics

7.1 Data mode operation

7.1.1 Frame structure

Table 7-1 summarizes the SHDSL frame structure. Complete bit definitions may be found in 7.1.2.

The size of each payload block is defined as k bits, where $k = 12 (i + n \times 8)$. The payload data rate is set by: $n \times 64 + i \times 8$ kbit/s, where $3 \leq n \leq 36$ and $0 \leq i \leq 7$. For $n = 36$, i is restricted to the values of 0 or 1. Note that optional extensions described in Annex F allow values of n up to 89. The value of i shall be negotiated during startup, and shall apply to all values of n. The selected value of i applies to all values of n, will be negotiated during pre-activation, and does not include the 8 kbit/s framing overhead.

In the optional M-pair mode, M separate PMS-TC sublayers are active – one for each wire pair. In this case, the above formula represents the payload data rate for each pair rather than the aggregate payload rate. All pairs shall operate at the same payload rate, and the transmitters for all pairs shall maintain frame alignment within specified limits. In the STU-C, the symbol clocks for each pair shall be derived from a common source. The maximum differential delay between the start of STU-C frames shall be no greater than four (4) symbols at the line side of each SHDSL transmitter. In the STU-R, symbol clocks may be derived from loop timing on each pair, so these clocks shall be locked in frequency but shall have an arbitrary phase relationship. The maximum differential delay between the start of STU-R frames shall be no greater than six (6) symbols at the line side of each SHDSL transmitter.

Table 7-1/G.991.2 – SHDSL frame structure

Time	Frame bit #	Over-head bit #	Name	Description	Notes
0 ms	1-14	1-14	*sw*1-*sw*14	Frame Sync Word	
	15	15	*fbit*1/*losd*	Fixed Indicator bit #1 (Loss of Signal)	
	16	16	*fbit*2/*sega*	Fixed Indicator bit #2 (Segment Anomaly)	
	17 → k + 16	--------	*b*1	Payload block #1	
	k + 17	17	*eoc*01	EOC bit #1	
	k + 18	18	*eoc*02	EOC bit #2	
	k + 19	19	*eoc*03	EOC bit #3	
	k + 20	20	*eoc*04	EOC bit #4	
	k + 21	21	*crc*1	Cyclic Redundancy Check #1	CRC-6
	k + 22	22	*crc*2	Cyclic Redundancy Check #2	CRC-6
	k + 23	23	*fbit*3/*ps*	Fixed Indicator bit #3 (Power Status)	
	k + 24	24	*sbid*1	Stuff bit ID #1	Spare in synchronous mode

Table 7-1/G.991.2 – SHDSL frame structure

Time	Frame bit #	Over-head bit #	Name	Description	Notes
	k + 25	25	*eoc*05	EOC bit #5	
	k + 26	26	*eoc*06	EOC bit #6	
	k + 27 → 2k + 26	--------	*b*2	Payload block #2	
	2k + 27	27	*eoc*07	EOC bit #7	
	2k + 28	28	*eoc*08	EOC bit #8	
	2k + 29	29	*eoc*09	EOC bit #9	
	2k + 30	30	*eoc*10	EOC bit #10	
	2k + 31	31	*crc*3	Cyclic Redundancy Check #3	CRC-6
	2k + 32	32	*crc*4	Cyclic Redundancy Check #4	CRC-6
	2k + 33	33	*fbit*4/*segd*	Fixed Indicator bit #4 (Segment Defect)	
	2k + 34	34	*eoc*11	EOC bit #11	
	2k + 35	35	*eoc*12	EOC bit #12	
	2k + 36	36	*sbid*2	Stuff bit ID #2	Spare in synchronous mode
	2k + 37 → 3k + 36	--------	*b*3	Payload block #3	
	3k + 37	37	*eoc*13	EOC bit #13	
	3k + 38	38	*eoc*14	EOC bit #14	
	3k + 39	39	*eoc*15	EOC bit #15	
	3k + 40	40	*eoc*16	EOC bit #16	
	3k + 41	41	*crc*5	Cyclic Redundancy Check #5	CRC-6
	3k + 42	42	*crc*6	Cyclic Redundancy Check #6	CRC-6
	3k + 43	43	*eoc*17	EOC bit #17	
	3k + 44	44	*eoc*18	EOC bit #18	
	3k + 45	45	*eoc*19	EOC bit #19	
	3k + 46	46	*eoc*20	EOC bit #20	
6 – 3/ (k + 12) ms	3k + 47 → 4k + 46	--------	*b*4	Payload block #4	
	4k + 47	47	*stb*1	Stuff bit #1	Vendor dependent in synchronous mode
6 ms nominal	4k + 48	48	*stb*2	Stuff bit #2	Vendor dependent in synchronous mode
	4k + 49	49	*stb*3	Stuff bit #3	Not present in synchronous mode
6 + 3/ (k + 12) ms	4k + 50	50	*stb*4	Stuff bit #4	Not present in synchronous mode

7.1.2 Frame bit definitions

In Table 7-1, the bit sequence of the SHDSL frame (prior to scrambling at the transmit side and after descrambling at the receive side) is presented. The frame structures are identical in both upstream and downstream directions of transmission. Spare bits in either direction shall be set to 1.

The following frame bit definitions are used:

7.1.2.1 *sw*1 – *sw*14 (Frame Sync Word)

The frame synchronization word (FSW) enables SHDSL receivers to acquire frame alignment. The FSW (bits *sw*1 – *sw*14) is present in every frame and is specified independently for the upstream and downstream directions.

7.1.2.2 *b*1 – *b*4 (Payload Blocks)

Used to carry user data. The internal structure of the payload blocks is defined in 8.1.

7.1.2.3 *eoc*01 – *eoc*20 (Embedded Operations Channel)

20 bits (*eoc*01... *eoc*20) are provided as a separate maintenance channel. See 9.5 for details. In *M*-pair mode, *eoc*01 – *eoc*20 on Pair 1 shall carry the primary EOC data. The corresponding Pair 2 to Pair *M* *eoc* bits shall be duplicates of the Pair 1 *eoc* bits.

7.1.2.4 *crc*1 – *crc*6 (Cyclic Redundancy Check code)

Six bits assigned to a cyclic redundancy check (CRC) code (see 7.1.3).

7.1.2.5 *fbit*1 – *fbit*4 (Fixed Indicator bits)

Used for the indication of time-critical framing information. Specific bit definitions are given below.

7.1.2.5.1 *fbit*1 = *losd* (Loss of Signal)

Used to indicate the loss of signal from the application interface. Loss of Signal = 0, Normal = 1. Definition of the conditions causing the indication of *losd* is vendor specific and beyond the scope of this Recommendation. In *M*-pair mode, *losd* on Pair 1 shall carry the primary *losd* indication. The *losd* bit on all other pairs shall be duplicates of the Pair 1 bit.

7.1.2.5.2 *fbit*2 = *sega* (Segment Anomaly)

Used to indicate a CRC error on the incoming SHDSL frame. A segment anomaly indicates that a regenerator operating on a segment has received corrupted data and therefore the regenerated data is unreliable. The purpose of segment anomaly is to ensure internal performance monitoring integrity; it is not intended to be reported to an external management entity. CRC Error = 0, Normal = 1.

7.1.2.5.2.1 STU operation

The STU shall set the *sega* bit to 1.

7.1.2.5.2.2 SRU operation

If a CRC error is declared for an incoming frame, an SRU shall set the *sega* bit to 0 in the next available outgoing frame in the forward direction, i.e., in the direction of the data over which the CRC error was observed. If no CRC error is declared, then an SRU shall pass the *sega* bit without modification.

7.1.2.5.3 *fbit*3 = *ps* (Power Status)

The power status bit *ps* is used to indicate the status of the local power supply in the STU-R. The power status bit is set to 1 if power is normal and to 0 if the power has failed. On loss of power at the STU-R, there shall be enough power left to send the *ps* bit in at least one and preferably three consecutive frames towards the STU-C. Note that, in the event of a power failure, the *ps* bit should be set to 0 for as many frames as possible before deactivation. If the *ps* bit is set for less than three frames, it is up to the application at the STU-C to determine the validity of the message. Regenerators shall pass this bit transparently. In *M*-pair mode, *ps* on Pair 1 shall carry the primary power status indication. The *ps* bit on all other pairs shall be duplicates of the Pair 1 *ps* bit.

7.1.2.5.4 *fbit*4 = *segd* (Segment Defect)

Used to indicate a loss of sync on the incoming SHDSL frame. A segment defect indicates that a regenerator has lost synchronization and therefore the regenerated data is unavailable. This bit is typically reported to an external management entity and is used to ensure timely protection switching, alarm filtering, etc. Loss of Sync = 0, Normal = 1.

7.1.2.5.4.1 STU operation

The STU shall set the *segd* bit to 1.

7.1.2.5.4.2 SRU operation

If a LOSW-Defect is declared, an SRU shall set the *segd* bit to 0 in the next available outgoing frame in the forward direction, i.e., in the direction of the data over which the LOSW-Defect was observed. If no LOSW-Defect is declared, then an SRU shall pass the *segd* bit without modification.

7.1.2.6 *sbid*1, *sbid*2 (Stuff Indicator bits)

In plesiochronous mode, the stuff indicator bits indicate whether or not a stuffing event occurs in the frame. Both bits shall be set to 1 if the four stuff bits are present at the end of the current frame. Both bits shall be set to 0 if there are no stuff bits at the end of the current frame. In synchronous mode, *sbid*1 and *sbid*2 are spare bits.

7.1.2.7 *stb*1 – *stb*4 (Stuffing Bits)

In plesiochronous mode, these bits are used together. Either zero or four stuffing bits are inserted, depending on the relation of the timing between the upstream and downstream channels. In synchronous framing mode, *stb*1 and *stb*2 are present in every frame, and *stb*3 and *stb*4 are not present. The values of *stb*1 – *stb*4 are specified independently for the upstream and downstream directions.

7.1.3 CRC Generation (*crc*1 … *crc*6)

A cyclic redundancy check (CRC) shall be generated for each frame and transmitted on the following frame. The six CRC bits (*crc*1 to *crc*6) shall be the coefficients of the remainder polynomial after the message polynomial, multiplied by D^6, is divided by the generating polynomial. The message polynomial shall consist of all bits in the frame except for the synchronization word, CRC bits, and the stuff bits. (There are thus $4k + 26$ message bits in a frame that are covered by the CRC check.) The message bits shall be ordered as in the frame itself, i.e., m_0 is the first bit, m_1 is the second bit, etc. The CRC check bits shall be calculated according to the equation:

$$crc(D) = m(D)D^6 \bmod g(D)$$

where:

$$m(D) = m_0 D^{4k+25} \oplus m_1 D^{4k+24} \oplus \ldots \oplus m_{4k+24} D \oplus m_{4k+25}$$

is the message polynomial,

$$g(D) = D^6 \oplus D \oplus 1$$

is the generating polynomial,

$$crc(D) = crc1D^5 \oplus crc2D^4 \oplus \ldots \oplus crc5D \oplus crc6$$

is the CRC check polynomial, ⊕ indicates modulo-2 addition (exclusive OR), and D is the delay operator.

7.1.4 Frame synchronization

In plesiochronous clocking mode, SHDSL uses a variable length PMS-TC frame and bit stuffing to synchronize the PMS-TC frame rate with the incoming payload rate. Quick acquisition of frame synchronization and the ability to maintain frame synchronization in the presence of errors are important properties of the frame structure.

Three types of bit fields are provided for use in frame synchronization: Frame Sync Word, Stuff Bits, and Stuff Bit IDs. The Frame Sync Word is 14 bits long and is present on every frame. The stuff bits are four contiguous bits which are present only at the end of long frames. Stuff Bit IDs are two bits distributed within the frame which indicate whether the current frame contains the four stuffing bits. These distributed bits provide improved immunity to frame alignment errors caused by burst errors.

The precise manner in which this information is used to acquire or maintain frame synchronization is the choice of the receiver designer. Since different frame synchronization algorithms may require different values for the bits of the FSW and Stuff Bits, a provision has been made to allow the receiver to inform the far end transmitter of the particular values that are to be used for these fields in the transmitted PMS-TC frame.

7.1.5 Scrambler

The scrambler in the STU-C and the STU-R transmitters shall operate as shown in Figures 7-1 and 7-2, respectively. In these figures, T_b indicates a delay of one bit duration and ⊕ is the binary exclusive-OR operation. The frame sync word bits and the stuff bits in the SHDSL data mode frame (Table 7-1) shall not be scrambled. While the frame sync word bits and stuff bits are present at *f(n)*, the scrambler shall not be clocked, and *f(n)* shall be directly connected to *s(n)*.

7.1.5.1 STU-C scrambler

The block diagram of the STU-C scrambler is shown in Figure 7-1.

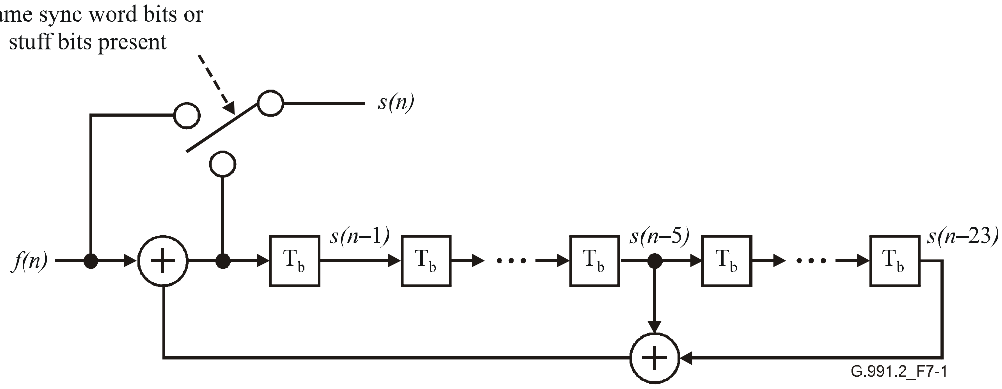


Figure 7-1/G.991.2 – Block diagram of the STU-C scrambler

7.1.5.2 STU-R scrambler

The block diagram of the STU-R scrambler is shown in Figure 7-2.

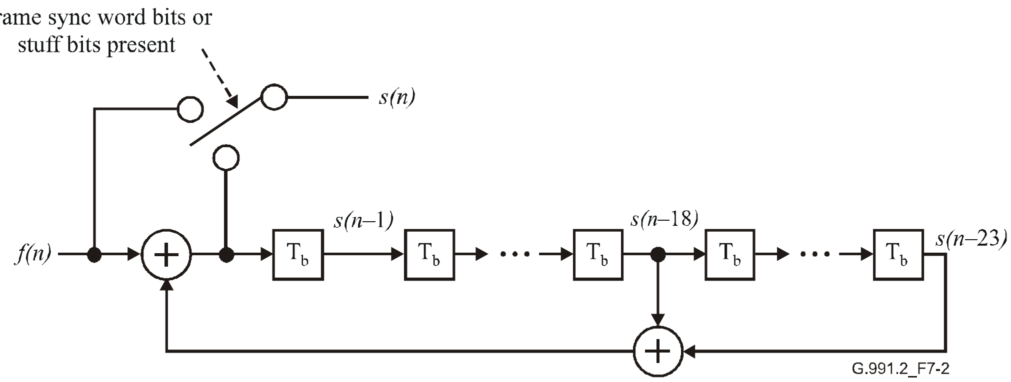


Figure 7-2/G.991.2 – Block diagram of the STU-R scrambler

7.1.6 Differential delay buffer

In the optional *M*-pair mode, it is understood that the characteristics of the *M* wire pairs may differ. Differences in wire diameter, insulation type, length, number and length of bridged taps and exposure to impairments may result in differences in transmission time between pairs. It is recommended that such differences in signal transfer delay between any two pairs be limited to a maximum of 50 µs at 150 kHz, corresponding to about 10 km difference in line length between STU-R and STU-C.

In transceivers supporting *M*-pair mode, a delay difference buffer shall be implemented to compensate for any difference in total transmission time of the SHDSL frames on different pairs. Such delay differences may be due to the pair differences described above, as well as to delays due to signal processing in the SHDSL transceivers in the STU-C, STU-R and possible signal regenerators. The function of this delay difference buffer is to align the SHDSL frames so that frames can be correctly reassembled. This buffer shall be capable of absorbing a delay difference of at least 6 symbols + 50 µs at the line side of each SHDSL receiver.

7.2 PMS-TC activation

7.2.1 Activation frame

The format of the activation frame is shown in Table 7-2. A T_c or T_r signal shall be generated by repetitively applying the activation frame information shown in Table 7-2 to the STU scrambler as shown in Figure 6-5. The activation frame contents shall be constant during the transmission of T_c and T_r. The activation frame sync bits are not scrambled, so they shall be applied directly to the uncoded 2-PAM constellation. The total number of bits in the activation frame is 4227. The activation frame shall be sent starting with bit 1 and ending with bit 4227.

In the optional *M*-pair mode, activation shall proceed in parallel on each of the *M* wire pairs.

Table 7-2/G.991.2 – Activation frame format

Activation frame bit LSB:MSB	Definition
1:14	Frame Sync for T_c and T_r: 11111001101011_2, where the left-most bit is sent first in time
	Frame Sync for F_c: 11010110011111_2, where the left-most bit is sent first in time
15:36	Precoder Coefficient 1: 22 bit signed two's complement format with 17 bits after the binary point, where the LSB is sent first in time
37:58	Precoder Coefficient 2
59:3952	Precoder Coefficients 3-179
3953:3974	Precoder Coefficient 180
3975:3995	Encoder Coefficient A: 21 bits where the LSB is sent first in time
3996:4016	Encoder Coefficient B: 21 bits where the LSB is sent first in time
4017:4144	Vendor Data: 128 bits of proprietary information
4145:4146	*M*-pair mode: STU-C: Number of wire pairs/STU-R: Ordering of wire pairs
4147:4211	Reserved: 65 bits set to logical zeros
4212:4227	CRC: c_1 sent first in time, c_{16} sent last in time

7.2.1.1 Frame sync

The frame sync for T_c and T_r is a 14-bit code. In binary, the code shall be 11111001101011, and shall be sent from left to right. For F_c, the frame sync shall be 11010110011111, or the reverse of the frame sync for T_c and T_r.

7.2.1.2 Precoder coefficients

The precoder coefficients are represented as 22-bit two's complement numbers, with the five most significant bits representing integer numbers from −16 (10000) to +15 (01111), and the remaining 17 bits are the fractional bits. The coefficients are sent sequentially, starting with coefficient C_1 and ending with coefficient C_N (from Figure 6-4), and the least significant bit of each coefficient is sent first in time. The minimum number of precoder coefficients shall be 128 and the maximum number shall be 180. If fewer than 180 precoder coefficients are used, the remaining bits in the field shall be set to zero.

7.2.1.3 Encoder coefficients

Referring to Figure 6-3, the coefficients for the programmable encoder are sent in the following order: a_0 is sent first in time, followed by a_1, a_2, … , and b_{20} is sent last in time.

7.2.1.4 Vendor data

These 128 bits are reserved for vendor-specific data.

7.2.1.5 *M*-pair mode: Ordering of wire pairs

In the optional *M*-pair mode these two bits are used to define the order of the *M* wire pairs. They are used to determine how user data is split into *M* loops at the transmitter and combined in the receiver as specified in 7.1.1. The assignment of loop 1 to loop *M* is vendor-specific.

Bits 4145 to 4146 in the activation frame of the STU-C device are used to specify the number *M* of wire pairs. LSB first. $M = 1$: 00_2; $M = 2$: 10_2; $M = 3$: 01_2; $M = 4$: 11_2. This activation frame entry is identical on all *M* wire pairs.

Bits 4145 to 4146 of the activation frame of the STU-R device are used to identify the ordinal number of each of the *M* wire pairs. LSB first. Wire pair 1: 00_2; wire pair 2: 10_2; wire pair 3: 01_2; wire pair 4: 11_2. This activation frame entry is different on each of the *M* wire pairs.

If the system is not operating in *M*-pair mode, these two bits shall be set to logical zeros. In four-wire mode, the ordinal numbers are assigned as described in 6.3, and bits 4145 to 4146 of the activation frame shall be set to zero.

7.2.1.6 Reserved

These 65 bits are reserved for future use and shall be set to logical zeros.

7.2.1.7 CRC

The sixteen CRC bits (c_1 to c_{16}) shall be the coefficients of the remainder polynomial after the message polynomial, multiplied by D^{16}, is divided by the generating polynomial. The message polynomial shall be composed of the bits of the activation frame, where m_0 is bit 15 and m_{4196} is bit 4211 of the activation frame, such that:

$$crc(D) = m(D)D^{16} \bmod g(D)$$

where:

$$m(D) = m_0 D^{4196} \oplus m_1 D^{4195} \oplus \ldots \oplus m_{4195} D \oplus m_{4196}$$

is the message polynomial,

$$g(D) = D^{16} \oplus D^{12} \oplus D^5 \oplus 1$$

is the generating polynomial,

$$crc(D) = c_1 D^{15} \oplus c_2 D^{14} \oplus \ldots \oplus c_{15} D \oplus c_{16}$$

is the CRC check polynomial, $\oplus$ indicates modulo-2 addition (exclusive OR), and *D* is the delay operator.

7.2.2 Activation scrambler

The scrambler in the STU-C and the STU-R transmitters (see Figure 6-5) shall operate as shown in Figures 7-1 and 7-2, where T_b is a delay of one bit duration, and $\oplus$ is binary exclusive-OR. The frame sync bits in the activation frame shall not be scrambled. While the frame sync bits are present at *f(n)*, the scrambler shall not be clocked, and *f(n)* shall be directly connected to *s(n)*.

8 TPS-TC layer functional characteristics

8.1 Payload block data structure

Each payload block shall consist of 12 Sub-blocks, and shown in Figure 8-1. The size of each payload sub-block is defined as k_s, where $k_s = i + n \times 8$ [bits]. As stated in 7.1, the payload data rate is set by: $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For $n = 36$, i is restricted to the values of 0 or 1. Note that optional extensions described in Annex F allow values of *n* up to 89. All structure of data within payload sub-blocks (i.e., support for clear broadband channels, subchannels, and region-specific services) is specified in Annex E.

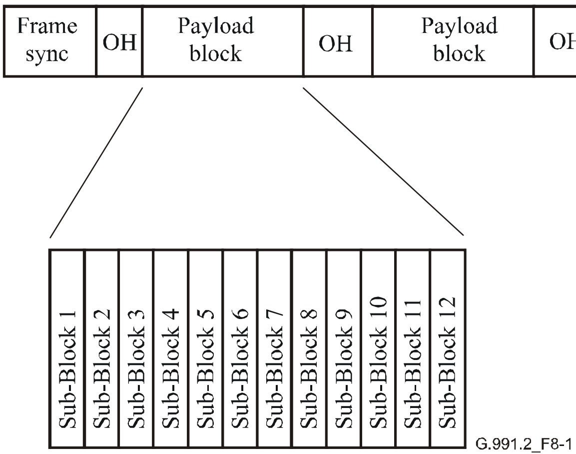


Figure 8-1/G.991.2 – Structure of payload blocks

8.2 Data interleaving in *M*-pair mode

In the optional M-pair mode, interleaving of payload data between pairs is necessary. This shall be accomplished by interleaving within payload sub-blocks among all pairs. k_s bits in each sub-block shall be carried on Pair 1, and an additional k_s bits shall be carried on each of the other pairs, as shown in Figure 8-2 for the case of $M = 2$. The size of each payload sub-block is defined as $M \times k_s$, where $k_s = i + n \times 8$. As stated in 7.1, the payload data rate per pair is set by: $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For $n = 36$, i is restricted to the values of 0 or 1. Note that optional extensions described in Annex F allow values of n up to 89. All structure of data within payload sub-blocks (i.e., support for clear broadband channels, subchannels, and region-specific services) is specified in Annex E.

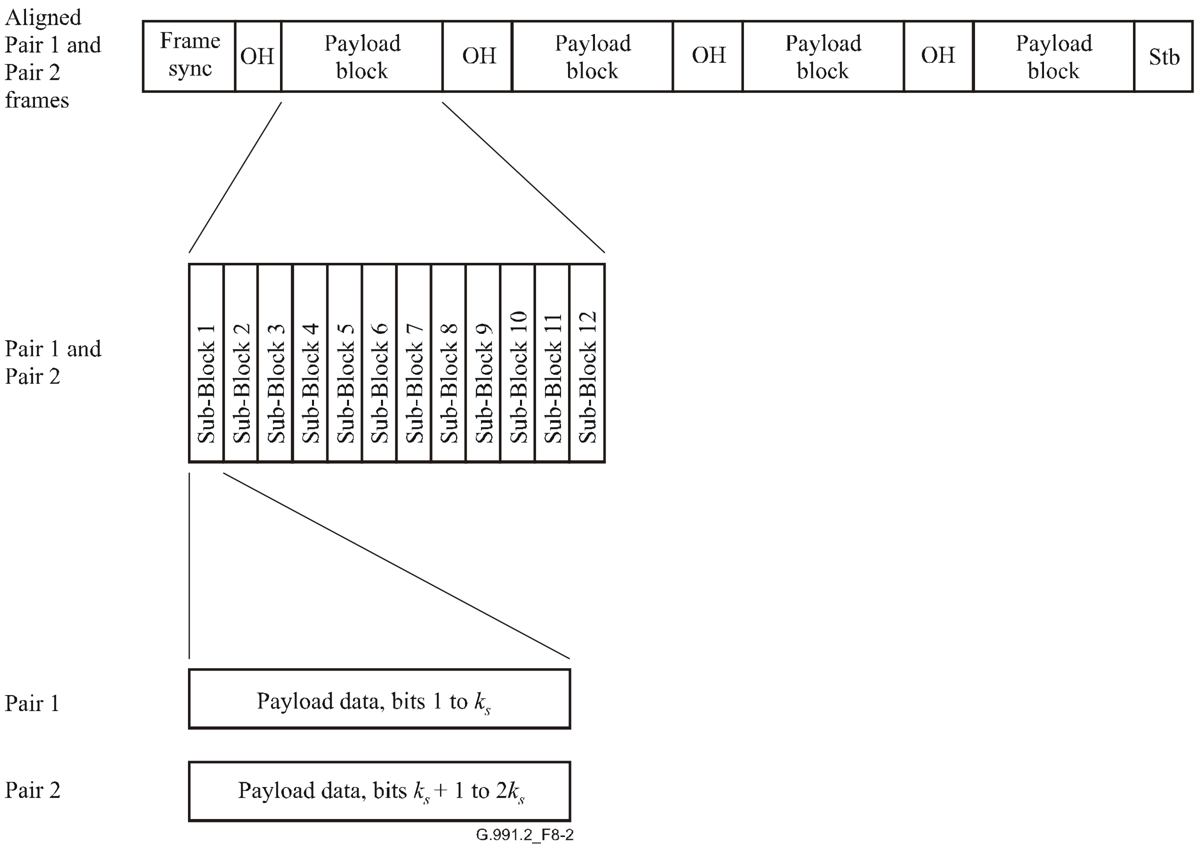
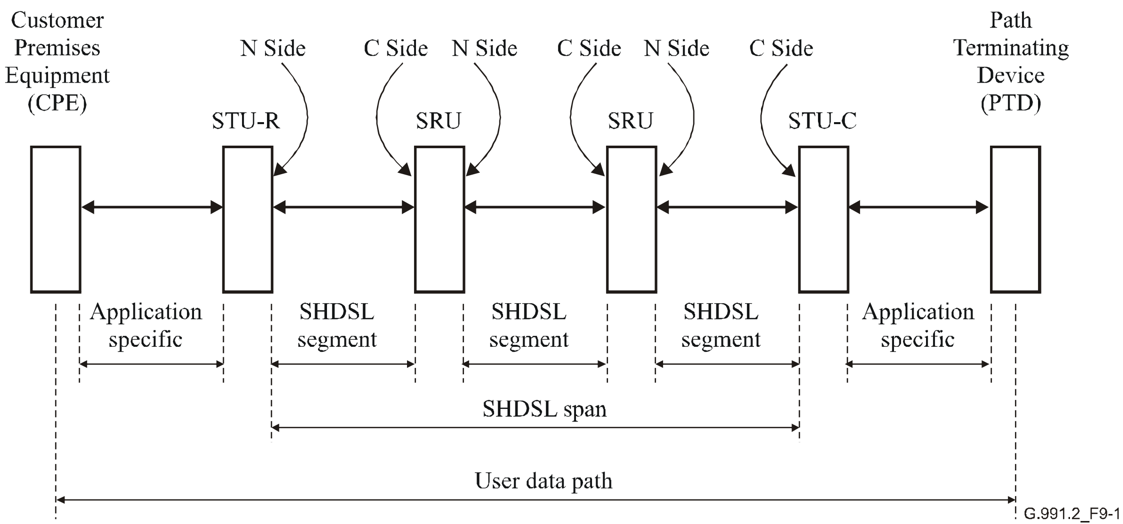


Figure 8-2/G.991.2 – Data interleaving within payload blocks

9 Management

9.1 Management reference model



NOTE – N = Network, C = Customer.

Figure 9-1/G.991.2 – Management reference model

Figure 9-1 shows the Management Reference Model for user data transport over SHDSL. This example includes two regenerator units for informative purposes. The presence of two regenerators is not intended to be a requirement or limit. An SHDSL segment is characterized by a metallic transmission medium utilizing an analogue coding algorithm, which provides both analogue and digital performance monitoring at the segment entity. An SHDSL segment is delimited by its two end points, known as segment terminations. An SHDSL segment termination is the point at which the analogue coding algorithms end and the subsequent digital signal is monitored for integrity.

All SHDSL performance monitoring data is transported over the EOC. The fixed indicator bits in the SHDSL frame are used for rapid communication of interface or SHDSL segment defects, which may lead to protection switching. In addition, the fixed indicator bits may be used for rapid alarm filtering SHDSL segment failures.

9.2 SHDSL performance primitives

9.2.1 Cyclical Redundancy Check Anomaly (CRC Anomaly)

A CRC anomaly shall be declared when the CRC bits generated locally on the data in the received SHDSL frame do not match the CRC bits (*crc*1 – *crc*6) received from the transmitter. A CRC anomaly only pertains to the frame over which it was declared.

9.2.2 Segment Anomaly (SEGA)

An upstream segment anomaly shall be declared when any SRU declares a CRC anomaly for an SHDSL frame moving in the direction from STU-R to STU-C. A downstream segment anomaly shall be declared when any SRU declares a CRC anomaly for an SHDSL frame moving in the direction from STU-C to STU-R. A segment anomaly indicates that a regenerator operating on a segment has received corrupted data and therefore the regenerated data is unreliable. The purpose of segment anomaly is to ensure internal SHDSL PMD integrity; it is not intended to be reported to an external management entity. A segment anomaly is indicated via the *sega* bit in the SHDSL frame (7.1.2.5.2).

9.2.3 Loss of Sync Defect (LOSW defect)

In plesiochronous mode, an LOSW defect shall be declared when at least three consecutive received frames contain one or more errors in the framing bits. The term framing bits shall refer to that portion of Frame Sync Word, Stuff Bits and Stuff Bit Ids, which are used for frame synchronization. An LOSW defect shall be cleared when at least two consecutive received frames contain no errors in the framing bits.

In synchronous mode, an LOSW defect shall be declared when at least three consecutive received frames contain one or more bit errors in the Frame Sync Word. An LOSW defect shall be cleared when at least two consecutive received frames contain no errors in the Frame Sync Word.

9.2.4 Segment Defect (SEGD)

An upstream segment defect shall be declared when any SRU declares a LOSW defect for data moving in the direction from STU-R to STU-C. A downstream segment defect shall be declared when any SRU declares a LOSW defect for data moving in the direction from STU-C to STU-R. A segment defect indicates that a regenerator has lost SHDSL synchronization and therefore the regenerated data is unavailable. A segment defect shall be cleared when all SRUs have no LOSW defects. This primitive is typically reported to an external management entity and is used to ensure timely protection switching, alarm filtering, etc. A segment defect is indicated via the *segd* bit in the SHDSL frame (7.1.2.5.4).

9.2.5 Loop attenuation defect

A Loop Attenuation Defect shall be declared when the observed Loop Attenuation is at a level higher than the configured threshold (9.5.5.7.5).

9.2.6 SNR margin defect

An SNR Margin Defect shall be declared when the observed SNR Margin is at a level lower than the configured threshold (9.5.5.7.5). SNR Margin is defined as the maximum dB increase in equalized noise or the maximum dB decrease in equalized signal that a system can tolerate and maintain a BER of 10^{-7}.

9.2.7 Loss of Sync Word Failure (LOSW failure)

An LOSW failure shall be declared after 2.5 ± 0.5 s of contiguous LOSW defect. The LOSW failure shall be cleared when the LOSW defect is absent between 2 and 20 s. The minimum hold time for indication of LOSW failure shall be 2 s.

9.3 SHDSL line related performance parameters

9.3.1 Code Violation (CV)

The SHDSL parameter Code Violation is defined as a count of the SHDSL CRC anomalies occurring during the accumulation period. This parameter is subject to inhibiting – see 9.3.6.

9.3.2 Errored Second (ES)

The SHDSL parameter Errored Second is defined as a count of 1-second intervals during which one or more CRC anomalies are declared and/or one or more LOSW defects are declared. This parameter is subject to inhibiting – see 9.3.6.

9.3.3 Severely Errored Second (SES)

The SHDSL parameter Severely Errored Second is defined as a count of 1-second intervals during which at least 50 CRC anomalies are declared or one or more LOSW defects are declared. (50 CRC anomalies during a 1-second interval is equivalent to a 30% errored frame rate for a nominal frame length.) This parameter is subject to inhibiting – see 9.3.6.

9.3.4 LOSW Second (LOSWS)

The SHDSL parameter LOSW Second is defined as a count of 1-second intervals during which one or more SHDSL LOSW defects are declared.

9.3.5 Unavailable Second (UAS)

The SHDSL parameter Unavailable Second is a count of 1-second intervals for which the SHDSL line is unavailable. The SHDSL line becomes unavailable at the onset of 10 contiguous SESs. The 10 SESs are included in the unavailable time. Once unavailable, the SHDSL line becomes available at the onset of 10 contiguous seconds with no SESs. The 10 s with no SESs are excluded from unavailable time.

9.3.6 Inhibiting rules

– UAS parameter counts shall not be inhibited.

– ES and SES shall be inhibited during UAS. Inhibiting shall be retroactive to the onset of unavailable time and shall end retroactively to the end of unavailable time.

– The CV parameter shall be inhibited during SES.

Further information on inhibiting rules and how ES and SES are decremented can be found in IETF RFC 2495: Definitions of Managed Objects for the DS1, E1, DS2 and E2 Interface Types [B9].

9.4 Performance data storage

In order to support SHDSL performance history storage at the STU-C, each SHDSL network element shall monitor performance and maintain a modulo counter for each performance parameter that is specified in 9.5.5.7.14 and 9.5.5.7.15, as appropriate. No initialization of these modulo counters is specified or necessary. By comparing the current reading of the modulo counter with the previous reading stored in memory, the data base manager in the STU-C can determine the number of counts to add to the appropriate performance history bin. (Note that the number of counts may decrease under some fault conditions – see 9.3 for additional information.) The modulo counters are reported in the SHDSL Performance Status Messages (9.5.5.7.14 and 9.5.5.7.15).

The STU-C shall collect performance history by polling each SHDSL network element with a time interval that precludes overflow of the modulo counter. For example, the modulo counter for Errored Seconds is 8 bits which allows a maximum of 255 s between polls before overflow may occur. Note that the polling that is referred to herein is implemented by the internal database manager in the STU-C rather than an external network manager.

The STU-C shall maintain performance history bins for each SHDSL segment endpoint. The performance history bins shall include the total collected counts for the current 15-minute period, 32 previous 15-minute periods, current 24-hour period, and 7 previous 24-hour periods.

9.5 Embedded operations channel

9.5.1 Management reference model

The STU-C shall maintain a management information database for external access by network management or via craft interface.

Optionally, the STU-R may maintain a management information database, which can be locally accessed (through a craft interface). This is particularly useful when the STU-C, due to fault conditions, is unreachable via the EOC.

Access to the management information database from craft interfaces on attached units shall be provided through a virtual-terminal interface.

9.5.2 EOC overview and reference model

The EOC allows terminal units to maintain information about the span. There are two basic flows of data, differentiated by which terminal unit initiates the data flow (and subsequently stores the information for external access). The data flow initiating from the STU-C is mandatory. The data flow initiating from the STU-R is optional, but all units must respond to requests in either direction of data flow. In all cases the "master database" shall be stored at the STU-C and all conflicts shall be resolved in favour of the STU-C (i.e., the information at the STU-C takes precedence). The data flows are illustrated in Table 9-1 for a two regenerator link (Q denotes a query or command message, R denotes a response message). Up to eight regenerators are supported by the protocol definition. Asterisks denote optional message transmissions. A block diagram example of a link with two regenerators is shown in Figure 9-1.

Table 9-1/G.991.2 – Illustration of EOC flow with two regenerators

Messages from STU-C Msg(src,dest)	Messages from SRU1 Msg(src,dest)	Messages from SRU2 Msg(src,dest)	Messages from STU-R Msg(src,dest)
Q(1,3) →	→ Process		
Process ←	← R(3,1)		
Q(1,4) →	→ Forward →	→ Process	
Process ←	← Forward ←	← R(4,1)	
Q(1,2) →	→ Forward →	→ Forward →	→ Process
Process ←	← Forward ←	← Forward ←	← R(2,1)
		Process ←	← Q(2,3)*
		R(3,2) →	→ Process
	Process ←	← Forward ←	← Q(2,4)*
	R(4,2) →	→ Forward →	→ Process
Process ←	← Forward ←	← Forward ←	← Q(2,1)*
R(1,2) →	→ Forward →	→ Forward →	→ Process
* Indicates optional messages.			

The data link layer of SHDSL EOC checks the FCS and if valid passes the packet to the network layer. If the CRC is invalid the entire packet is ignored. The network layer consists of three possible actions: Process, Forward, and Ignore/Terminate. Process means that the source address and HDLC information field are passed on to the application layer. Forward means that the packet is sent onward to the next SHDSL element. (Note that only SRUs will forward packets.) Ignore/Terminate means that the HDLC packet is ignored and is not forwarded. An SRU may both process and forward a packet in the case of a broadcast message. If the segment is not active in the forwarding direction, the SRU shall discard the packet instead. When the segment is active in the forwarding direction, the maximum forwarding delay in an SRU shall be 300 ms. All retransmission and flow control is administered by the endpoints, the STUs.

To accommodate the dual data flows, SHDSL regenerators have dual addresses as shown in Table 9-1. One address is for communication with the STU-C and the other address is for communication with the STU-R. During Discovery, the STU-C and optionally the STU-R send discovery probe messages, which propagate across the span and allow the SRUs to be numbered via a hop count field in the message. This process is explained in detail below.

The SHDSL terminal units communicate unidirectionally and thus have only one address. The STU-C is assigned a fixed address of 1 and the STU-R is assigned a fixed address of 2. At power-up, each SRU is assigned the address of 0 for each direction. Under a LOSW failure condition, the SRU shall reset its source address to 0 for the direction in which the LOSW failure exists. The SRU source address shall be changed from 0 if and only if a discovery probe message is received and processed. In this way, a regenerator will only communicate in the direction of a database. For instance, if a regenerator receives a probe message from the STU-C and not from the STU-R, then its address will remain 0 in the direction towards the remote.

9.5.3 EOC startup

After loop activation, the SHDSL EOC goes through three initialization stages: Discovery, Inventory and Configuration. During Discovery, the STU-C and optionally the STU-R will learn if any mid-span regenerators exist and their addresses will be determined. During Inventory, the STU-C will poll each SRU and the STU-R to establish inventory information on each element for the terminal unit's database. (Similarly, the STU-R may poll each SRU and the STU-C to establish its own database, although this is optional.) During Configuration, the STU-C configures the STU-R and any SRUs for alarm thresholds, signal characteristics, etc. There is no enforcement of the order or time of the Inventory and Configuration phases; the initiating STU is in control.

Table 9-12 is an example of Discovery starting from the STU-C and then followed by an optional Discovery initiated by the STU-R. Although these are shown sequentially in this example, they are actually independent; it is not necessary for the STU-R to wait until it received the probe from the STU-C before initiating its own Discovery phase. The STU-R may send its probe as soon as its EOC is active. The Discovery Response contains the current hop count, the vendor ID, EOC version and an indication of LOSW in the forward direction (i.e., in the direction of EOC flow that is opposite to the direction that the Discovery Response is sent).

Table 9-2/G.991.2 – Illustration of EOC discovery phase

Messages from STU-C Msg(src,dest,h)	Messages from SRU1 Msg(src,dest,h)	Messages from SRU2 Msg(src,dest,h)	Messages from STU-R Msg(src,dest,h)
DP(1,0,0) →			
	← DR(3,1,1)		
	DP(0,0,1) →		
	← Forward ←	← DR(4,1,2)	
		DP(0,0,2) →	
	← Forward ←	← Forward ←	← DR(2,1,3)
			← DP(2,0,0)
		DR(3,2,1)→	
		← DP(4,0,1)	
	DR(4,2,2) →	→ Forward →	
	← DP(3,0,2)		
DR(1,2,3) →	→ Forward →	→ Forward →	
NOTE – h = hop count, DP = Discovery Probe, DR = Discovery Response.			

After the Initiator (STU-C and optionally STU-R) has received a Discovery Response message from an element, it shall then begin the Inventory phase for that particular element. This is accomplished by polling that particular element for its inventory information. After the Initiator has received the inventory information for a unit, it shall then begin the Configuration phase by sending the appropriate configuration information to the corresponding element. The Inventory and Configuration Phases operate independently for each responding terminal/regenerator unit.

To ensure interoperability, the behaviour of slave or responding units is carefully specified by this Recommendation. The particular method for handling dropped packets or no response is left to the discretion of the initiating STU.

Table 9-3 shows the EOC state table for the network side of an SRU. Note that an identical, but independent, state machine exists for the customer side of an SRU to support messages originating from the STU-R.

The state machine consists of three states: Offline, Discovery and EOC Online. The Offline state is characterized by LOSW failure (a loss of SHDSL sync). The Discovery state is characterized by an unknown address. Once the address is learned through the Discovery message, the SRU enters the EOC online or active state. At this point, the SRU will respond to inventory, configuration, maintenance, or other messages from the STU-C.

Table 9-3/G.991.2 – SRU network EOC state table

Offline state

Event	Action
Network LOSW = 0	EOC State = Discovery Ready

Discovery ready state

Event	Action
Network LOSW = 1	Network EOC Address = 0 Network EOC State = Offline
Discovery probe message received from the Network side	Increment Hop Count Set Network EOC address to Hop Count +2 Compose and present Discovery message to Customer side application layer Send Discovery Response to STU-C Network EOC State = EOC Online
Message with address not equal to unit's address received from the Network side.	Request forwarding of the message from the Customer side network layer
Message Forwarding Requested from Customer side	Send requested message toward Network if EOC not offline

EOC online state

Event	Action
Network LOSW = 1	Network EOC Address = 0 Network EOC State = Offline
Discovery message received from the Network side	Increment Hop Count Set Network EOC address to Hop Count +2 Compose and present Discovery message to Customer side application layer Send Discovery Response to STU-C
Message with broadcast destination address received from the Network side	Process the message Request the Customer side EOC network layer to forward the message
Message with unit's destination address or address 0 received from the Network side	Process the message
Message with address not equal to unit's address received from the Network side	Request forwarding of message from the Customer side network layer
Message forwarding requested from Customer side network layer	Send requested message toward Network if EOC not offline

9.5.4 Remote management access

The STU-C shall maintain the master management database for the entire SHDSL span. (An optional second database is maintained at the STU-R.) Other units are only required to store enough information to accurately send information via the EOC. The information contained in the master database shall be accessible from any SHDSL unit that has a craft port and from network management if it is available. The craft access is in the form of a virtual-terminal interface (or virtual-craft-port interface). This interface is defined so that it can be used by any attached unit to access the terminal screen of another unit on the same SHDSL span. Support for this feature is optional, with the exception of the STU-C, which shall support the "host" side of at least one remote terminal connection. (Whether this interface can be active simultaneously with local craft access to the STU-C is a vendor decision and beyond the scope of this Recommendation.) The virtual-terminal interface consists of connect, disconnect, keyboard, and screen messages. After a connection has been established, input characters from the craft port are sent in Keyboard data messages to the "host" unit. The host unit, in turn, shall send information in the form of ASCII text, ASCII control codes, and screen control functions in Screen messages, whose contents are transmitted back to the craft port. The host unit shall echo characters.

The method for determining that remote access through the local craft port is desired or should be terminated is vendor specific, and beyond the scope of this Recommendation. Whatever method is used, capability for transmitting all valid key sequences (ASCII characters and control codes) shall be provided.

9.5.5 EOC transport

The EOC shall be transported in the SHDSL frame in bits *eoc*1 through *eoc*20. Five octets are contained in each two SHDSL frames, with specified alignment. The least significant bit (LSB) of the octets are located in bits 1, 9, and 17 of the EOC bits in the first frame and bits 5 and 13 of the second frame; each octet is transmitted LSB first. Octet alignment across frames is achieved through detection of the alignment of the HDLC Sync pattern ($7E_{16}$).

For optional M-pair operation, each EOC message shall be sent in parallel such that redundant and identical messages are sent over all M loops.

9.5.5.1 EOC data format

Numerical data and strings are placed in the EOC with octet alignment. Data items that are not an integral number of octets have been packed together to minimize message sizes.

Numerical Fields shall be transmitted most significant octet first, least significant bit first within an octet. (This is consistent with "network octet ordering" as in IETF RFC 1662: PPP in HDLC-like Framing [4].)

Strings shall be represented in the data stream with their first character (octet) transmitted first. Strings shall be padded with spaces or terminated with a NULL (00_{16}) to fill the allocated field size. String fields are fixed length so characters after a NULL in a string data field are "don't care".

9.5.5.2 EOC frame format

The EOC channel shall carry messages in an HDLC-like format as defined in 6.3/G.997.1 [3]. The channel shall be treated as a stream of octets; all messages shall be an integral number of octets.

The frame format uses a compressed form of the HDLC header, as illustrated in Table 9-4. The destination address field shall be the least significant 4 bits of octet 1; the source address field shall occupy the most significant 4 bits of the same octet (the address field). There is no control field. One or more sync octets ($7E_{16}$) shall be present between each frame. Inter-frame fill shall be accomplished by inserting sync octets as needed. Discovery probe messages shall be preceded by at least 5 sync octets to assure proper detection of octet alignment. The Information Field contains exactly one Message as defined below. The maximum length of a frame shall be 75 octets, not including the sync pattern or any octets inserted for data transparency.

Table 9-4/G.991.2 – Frame format for SHDSL EOC

Octet #	MSB Contents	LSB	
	Sync pattern $7E_{16}$		
	Source address bits 7..4	Destination address bits 3..0	
1	Message ID per Table 9-6.		Information
2	Message Content – Octet 2		field
	…		…
L	Message Content – Octet L		…
	FCS octet 1		
	FCS octet 2		
	Sync pattern $7E_{16}$		

9.5.5.3 Data transparency

Transparency for the information payload to the sync pattern ($7E_{16}$) and the control escape pattern $7D_{16}$ shall be achieved by octet stuffing.

Before transmission:

- octet pattern $7E_{16}$ is encoded as two octets $7D_{16}$, $5E_{16}$;
- octet pattern $7D_{16}$ is encoded as two octets $7D_{16}$, $5D_{16}$.

At reception:

- octet sequence $7D_{16}$, $5E_{16}$ is replaced by octet $7E_{16}$;
- octet sequence $7D_{16}$, $5D_{16}$ is replaced by octet $7D_{16}$;
- any other two-octet sequence beginning with $7D_{16}$ aborts the frame.

9.5.5.4 Frame check sequence

The frame check sequence (FCS) shall be calculated as specified in IETF RFC 1662 [4]. (Note that the FCS is calculated before data transparency.) The FCS shall be transmitted as specified in IETF RFC 1662.

9.5.5.5 Unit addresses

Each unit uses one source and destination address when communicating with upstream units and a separate, independent source and destination address when communicating with downstream units. Each address shall have a value between 0_{16} and F_{16}. Units shall be addressed in accordance with Table 9-5. Address F_{16} may only be used as a destination address and shall specify that the message is addressed to all units. Address 0_{16} is used to address the next attached or adjacent unit.

Table 9-5/G.991.2 – Device addresses

Address ($Base_{16}$)	Device
0	Adjacent device
1	STU-C
2	STU-R
3-A	Regenerators 1-8
B-E	Reserved (D and E not allowed)
F	Broadcast message, to all stations

NOTE – This Recommendation is not intended to indicate how many regenerators can or should be supported by a product; only how to identify them if they exist.

9.5.5.6 Message IDs

Table 9-6 summarizes message ID. Message IDs are listed as decimal numbers. Messages 0-64 represent request messages. Messages 128-192 represent messages that are sent in response to request messages. Each request message is acknowledged with the corresponding response. Request/Response Message IDs usually differ by an offset of 128.

Table 9-6/G.991.2 – Summary of message IDs

Message ID (decimal)	Message type	Initiating unit	Reference
0	Reserved		
1	Discovery Probe	STU-C, STU-R*, SRU	9.5.5.7.1
2	Inventory Request	STU-C, STU-R*	9.5.5.7.3
3	Configuration Request – SHDSL	STU-C	9.5.5.7.5
4	Reserved for Application Interface Configuration		
5	Configuration Request – Loopback Timeout	STU-C, STU-R*	9.5.5.7.6
6	Virtual Term. Connect Req.	STU-R*, SRU*	9.5.5.7.16
7	Virtual Terminal Disc. Req.	STU-R*, SRU*	9.5.5.7.16
8	Keyboard data message	STU-R*, SRU*	9.5.5.7.17
9	Maintenance request – System Loopback	STU-C, STU-R*	9.5.5.7.18
10	Maintenance request – Element Loopback	STU-C, STU-R*	9.5.5.7.19
11	Status Request	STU-C, STU-R*	9.5.5.7.11
12	Full Status Request	STU-C, STU-R*	9.5.5.7.12

Table 9-6/G.991.2 – Summary of message IDs

Message ID (decimal)	Message type	Initiating unit	Reference
13-14	Reserved		
15	Soft restart/Power backoff disable Request	STU-C	9.5.5.7.21
16	Reserved (Future)		
17	ATM Cell Status Request	STU-C, STU-R*	E.9.4.7
18	STU-R Configuration Request – Management	STU-C	9.5.5.7.9
19	Reserved for Voice Transport Request (Future)	Undefined	
20	ISDN Request	STU-C, STU-R	E.8.7.1, E.13.3
21	LAPV5 POTS and ISDN Setup Request	STU-C	E.13.6
22	Deactivation Request	STU-C, STU-R	H.1.3.1
23	Mapping Request	STU-C, STU-R*	9.5.5.7.27
23-63	Reserved (Future)		
64-88	Reserved for Line management Request	Undefined	9.5.5.7.22
89-111	Reserved		
112-119	Proprietary Message	Undefined	9.5.5.7.23
120	External Message	Undefined	9.5.5.7.24
121	G.997.1 Message	STU-C*, STU-R*	9.5.5.7.25
122-124	Reserved		
125-127	Excluded ($7D_{16}$, $7E_{16}$, $7F_{16}$)		
128	Reserved		
129	Discovery Response	All	9.5.5.7.2
130	Inventory Response	All	9.5.5.7.4
131	Configuration Response – SHDSL	STU-R, SRU	9.5.5.7.7
132	Reserved for Application Interface Configuration		
133	Configuration Response – Loopback Timeout	All	9.5.5.7.8
134	Virtual Terminal Connect Response	STU-C, SRU*, STU-R*	9.5.5.7.16
135	Reserved		
136	Screen data message	STU-C, SRU*, STU-R*	9.5.5.7.17
137	Maintenance Status	All	9.5.5.7.20
138	Reserved		
139	Status/SNR	All	9.5.5.7.13
140	Performance Status SHDSL Network Side	SRU, STU-R	9.5.5.7.14

Table 9-6/G.991.2 – Summary of message IDs

Message ID (decimal)	Message type	Initiating unit	Reference
141	Performance Status SHDSL Customer Side	STU-C, SRU	9.5.5.7.15
142	Reserved for Application Interface Performance		
143	Reserved (Future)		
144	Generic Unable to Comply (UTC)		9.5.5.7.26
145	ATM Cell Status Information	All	E.9.4.8
146	Configuration Response – Management	STU-R, SRU	9.5.5.7.10
147	Reserved for Voice Transport Response (Future)	Undefined	
148	ISDN Response	STU-C, STU-R	E.8.7.1, E.13.3
149	LAPV5 POTS and ISDN Set-up	STU-R	E.13.6
150	Deactivation Response	STU-C, STU-R	H.1.3.2
151	Mapping Response	All	9.5.5.7.28
152-191	Reserved (Future)		
192-216	Segment Management Response (reserved)	Undefined	9.5.5.7.22
217-239	Reserved (Future)		
240-247	Proprietary message Response	Undefined	9.5.5.7.23
248-252	Reserved		
253-255	Excluded (FD_{16}, FE_{16}, FF_{16})		
* Denotes optional support. A unit may initiate this message.			

9.5.5.7 Message contents

Each message shall have the contents in the format specified in Tables 9-7 through 9-31. If any message has a message length longer than expected and is received in a frame with a valid FCS, then the known portion of the message shall be used and the extra octets discarded. This will permit addition of new fields to existing messages and maintain backward compatibility. New data fields shall only be placed in reserved bits after the last previously defined data octet. Reserved bits and octets shall be filled with the value 00_{16} for forward compatibility.

Response messages may indicate UTC (Unable to Comply). Note that this is not an indication of non-compliance. UTC indicates that the responding unit was unable to implement the request.

9.5.5.7.1 Discovery probe – Message ID 1

The discovery probe message shall be assigned Message ID 1, and is used to allow an STU to determine how many devices are present and assign addresses to those units.

Table 9-7/G.991.2 – Discovery probe information field

Octet #	Contents	Data type	Reference
1	1	Message ID	
2	Hop Count	Unsigned char	9.5.3

9.5.5.7.2 Discovery response – Message ID 129

The discovery response message shall be assigned Message ID 129. This message shall be sent in response to a discovery probe message. The hop count field shall be set to 1 larger than the value received in the discovery probe message causing the response. (The full receive state machine is described in Table 9-3.) Forward LOSW indication means that the segment is down in the forward direction from the SRU. In the case of optional *M*-pair operation, Forward LOSW indication means that all M loops are down in the forward direction from the SRU. In either case, the SRU is unable to forward the Discovery Probe message to the adjacent unit and it reports this fact to the initiating STU. The Forward LOSW octet field shall be set to 00_{16} for responses from an STU.

The Vendor ID field is used to identify the system integrator, as specified in 9.5.5.7.4.

The SHDSL version number indicates the SHDSL standard to which the system was built. For the present version of this Recommendation (12/2003), these bits shall be set to 00001000.

The vendor EOC software version number shall be assigned by the system vendor as identified by the vendor ID. Software version numbers are to be incremented for each new SHDSL standard.

Table 9-8/G.991.2 – Discovery response information field

Octet #	Contents	Data type	Reference
1	129	Message ID	
2	Hop Count	Unsigned char	9.5.3
3	Reserved		
4-11	Vendor ID (ordered identically to bits in G.994.1 Vendor ID)		
12	Vendor EOC Software Version	Unsigned char	
13	SHDSL Version #	Unsigned char	
14 bits 7..1	Reserved		
14 bit 0	Forward LOSW indication, EOC unavailable	Bit	1 = Unavailable 0 = Available

9.5.5.7.3 Inventory request – Message ID 2

The inventory request message shall be assigned Message ID 2. This message is used to request an inventory response from a particular unit. It shall only be transmitted by STU devices. There shall be no octets of content for this message.

Table 9-9/G.991.2 – Inventory request information field

Octet #	Contents	Data type	Reference
1	2	Message ID	

9.5.5.7.4 Inventory response – Message ID 130

The inventory response message shall be assigned Message ID 130. This message shall be sent in response to an inventory request message.

The SHDSL version number indicates the SHDSL standard to which the system was built. For G.shdsl.*bis* (draft), these bits shall be set to 00001000.

The Vendor ID field is used to specify the system integrator. In this context, the system integrator usually refers vendor of the smallest field-replaceable unit. This typically is also the entity pointed to by the Unit Identification Code (CLEI™) Field. As such, the Vendor ID field contents may not be the same as the Vendor ID indicated within ITU-T Rec. G.994.1, which relates to the manufacturer of the physical layer interface. The serial number, model number, issue number, list number, and software revision number shall all be assigned with respect to the system integrator.

Special unit identification codes are used in North America. These CLEI (Common Language Equipment Identifier) codes are used by network service providers for inventory, spare-part ordering, provisioning and maintenance operations. In North America, CLEI codes are used as a vendor's product ID. CLEI codes conform to ANSI T1.213, Coded Identification of Equipment Entities of the North American Telecommunications System for Information Exchange. In regions outside North America, these fields may be set to zero.

Information on the modem software version, the vendor list (modem hardware version), the modem issue, the model number, and the modem serial number are specific to the system. Therefore, this information shall be assigned by the system vendor as identified by the vendor ID.

The vendor software version indicates the version of the software of the SHDSL system. The vendor software version is not necessarily identical to the EOC software version in 9.5.5.7.2. The vendor list number indicates the version number of the system hardware. The vendor issue field indicates the particular usage of the unit. The vendor model number is a unique number for the particular type of unit. The vendor serial number is a number that identifies every unit individually.

Table 9-10/G.991.2 – Inventory response information field

Octet #	Contents	Data type	Reference
1	130	Message ID	
2	SHDSL Version #	Unsigned char	
3-5	Vendor List #	3-octet string	
6-7	Vendor Issue #	2-octet string	
8-13	Vendor Software Version	6-octet string	
14-23	Unit Identification Code (CLEI™)	10-octet string	
24	Reserved		
25-32	Vendor ID (ordered identically to bits in G.994.1 Vendor ID)		
33-44	Vendor model #	12-octet string	
45-56	Vendor serial #	12-octet string	
57-68	Other vendor information	12-octet string	

9.5.5.7.5 Configuration request – SHDSL: Message ID 3

The configuration request – SHDSL message is transmitted by the STU-C to configure the SHDSL interface(s) of attached units. This message may be broadcast or addressed to specific units. It is acknowledged with a configuration response – SHDSL message. For SHDSL, SNR is measured internal to the transceiver decision device as opposed to the external segment termination. The "Off" setting indicates that threshold crossings are not reported. Loop attenuation and SNR margin are local alarms that are reported in Messages 140 and 141. In addition, these alarms may be physically indicated on the equipment. SHDSL loop attenuation shall be defined as follows:

$$LoopAtten_{SHDSL}(H) = \frac{2}{f_{sym}} \left(\int_0^{\frac{f_{sym}}{2}} 10\times\log_{10}\left[\sum_{n=0}^{1} S\left(f - nf_{sym}\right)\right] df - \int_0^{\frac{f_{sym}}{2}} 10\times\log_{10}\left[\sum_{n=0}^{1} S\left(f - nf_{sym}\right)\left|H\left(f - nf_{sym}\right)\right|^2\right] df \right)$$

where f_{sym} is the symbol rate, $\frac{1}{H(f)}$ is the insertion loss of the loop, and $S(f)$ is the nominal transmit PSD.

Table 9-11/G.991.2 – Configuration request – SHDSL information field

Octet #	Contents	Data type	Reference
1	3	Message ID	
2 bit 7	Config Type	Bit	0-normal, 1-Read only
2 bits 6..0	SHDSL Loop Attenuation threshold (dB)	Enumerated	0 = off, 1 to 127
3 bits 7..4	SHDSL SNR Margin threshold (dB)	Enumerated	0 = off, 1 to 15
3 bits 3..0	Reserved		Set to 0

9.5.5.7.6 Configuration request – loopback timeout: Message ID 5

The configuration request – loopback timeout message is transmitted by the STU-C (and optionally the STU-R) to set loopback timeouts for individual elements. If a loopback is not cleared before the expiration of the timeout, then the element shall revert to normal operation. This message may be broadcast or addressed to specific units. It is acknowledged with a configure response – loopback timeout message. If date and time information is sent in octets 4-21, then these strings shall conform to ISO 8601 [5]. If date and time information is not sent, then these fields shall be filled with zeros.

Table 9-12/G.991.2 – Configuration request – loopback timeout information field

Octet #	Contents	Data type	Reference
1	5	Message ID	
2 bit 7	Config Type	Bit	0 = normal, 1 = Read-only.
2 bits 6..4	Reserved		
2 bits 3..0-3	Loopback timeout	12-bit unsigned integer	In minutes, 0 = no timeout
4-13	YYYY-MM-DD	10-octet date string	ISO 8601
14-21	HH:MM:SS	8-octet time string	ISO 8601

9.5.5.7.7 Configuration response – SHDSL: Message ID 131

The configuration response – SHDSL message is transmitted to the STU-C in response to a configuration request – SHDSL message. This response is sent after the applicable configuration changes have been made. The values of the response shall be set to the new values, after they have been applied. If a transceiver unit is unable to comply with the request, the bit in the compliance octet is set and the current settings are reported. If the config request message was received with a config type of "Read-Only," then no changes are made to the current configuration and the current values are reported.

Table 9-13/G.991.2 – Configuration response – SHDSL information field

Octet #	Contents	Data type	Reference
1	131	Message ID	
2 bits 7..1	Reserved		
2 bit 0	UTC (Unable to Comply)	Bit	0 = OK, 1 = UTC
3	SHDSL Loop Attenuation threshold (dB)	Char	0 = off, 1 to 127
4 bits 7..4	SHDSL SNR Margin threshold (dB)	Enumerated	0 = off, 1 to 15
4 bits 3..0	Reserved		Set to 0

9.5.5.7.8 Configuration response – loopback timeout: Message ID 133

The configuration response – loopback timeout message is transmitted to acknowledge the configuration request – loopback timeout message. This response is sent after the applicable configuration changes have been made. The values of the response shall be set to the new values, after they have been applied. If a transceiver unit is unable to comply with the request, the bit in the compliance octet is set and the current settings are reported. If the config request message was received with a config type of "Read-Only," then no changes are made to the current configuration and the current values are reported.

Table 9-14/G.991.2 – System Loopback Timeout Response information field

Octet #	Information Field	Data type	Reference
1	133	Message ID	
2 bits 7..1	Reserved		
2 bit 0	UTC (Unable to Comply)	Bit	0 = OK, 1 = UTC
3 bits 7..4	Reserved		
3 bits 3..0-4	Loopback timeout	12-bit unsigned integer	In minutes, 0 = no timeout
5-14	YYYY-MM-DD	10-octet date string	ISO 8601 [5]
15-22	HH:MM:SS	8-octet time string	ISO 8601

9.5.5.7.9 STU-R config – management: Message ID 18

The config request – management message is transmitted by the STU-C to enable or disable STU-R initiated management flow. The destination address shall be F_{16} to indicate this is a broadcast message. STU-R initiated management flow is enabled by default. When disabled, an SRU shall not respond to any STU-R-initiated request messages, and the STU-R shall not issue any such messages (messages 2-12). Config type of Read-Only indicates that the addressed unit ignore the subsequent values in the message and report back its current configuration.

Table 9-14a/G.991.2 – Configuration request – management information field

Octet #	Contents	Data type	Reference
1	Message ID 18	Message ID	
2 bit 7	ConfigType	Bit	0-normal, 1-Read-Only
2 bits 6..1	Reserved		
2 bit 0	STU-R Initiated Management Flow	Bit	0-Enable, 1-Disabled

9.5.5.7.10 Config response – management message: Message ID 146

Config response – management message is sent by all units to acknowledge to the config request – management message.

Table 9-14b/G.991.2 – Configuration response – management information field

Octet #	Contents	Data type	Reference
1	Message ID 146	Message ID	
2 bits 7..1	Reserved		
2 bit 0	UTC (Unable to Comply)	Bit	0-OK, 1-UTC
3 bits 7..1	Reserved		
3 bit 0	STU-R Initiated Management Flow Status	Bit	0-Enabled, 1-Disabled

9.5.5.7.11 Status request – Message ID 11

The status request message is used to poll an element for alarm and general performance status.

The polled unit will respond with one or more of the following status response messages:

- Status/SNR response – 139 (9.5.5.7.13).
- SHDSL network side performance status – 140 (9.5.5.7.14).
- SHDSL customer side performance status – 141 (9.5.5.7.15).
- Maintenance status – 137 (9.5.5.7.20).

In the optional *M*-pair mode, messages 139, 140, and 141 contain status information that is specific to a particular pair. In this case, *M* messages each (one corresponding to each pair) of types 139, 140, and 141 may be sent by the polled unit in response to a status request message. The responding element shall provide the loop ID information in EOC messages 139, 140, and 141. The responding element shall first provide the information relating to loop 1, followed shortly thereafter with the requested information for loop 2 (if $M \geq 2$), then loop 3 (if $M \geq 3$), then loop 4 (if $M = 4$).

If active alarm, fault or maintenance conditions exist then the polled unit shall respond with the messages that correspond to the active conditions.

If there has been any change in performance status other than SNR margin since the last time a unit was polled, then the unit shall respond with the messages which contain the change in performance status.

Otherwise, the polled unit shall respond with the status/SNR response – 139 (9.5.5.7.13).

Table 9-15/G.991.2 – Status request information field

Octet #	Information field	Data type
1	Message ID 11	Message ID

9.5.5.7.12 Full status request – Message ID 12

The full status request message is used to poll an element for its complete current status. The following messages shall be sent in response to the full status request:

- SHDSL network side performance status (9.5.5.7.14).
- SHDSL customer side performance status (9.5.5.7.15).
- Maintenance status (9.5.5.7.20).

In the optional *M*-pair mode, the following messages shall be sent in response to the full status request:

- SHDSL network side performance status (9.5.5.7.14) – related to Loop 1.
- SHDSL network side performance status – for Loop 2 to Loop *M* (one message per loop).
- SHDSL customer side performance status (9.5.5.7.15) – related to Loop 1.
- SHDSL customer side performance status – for Loop 2 to Loop *M* (one message per loop).
- Maintenance status (9.5.5.7.20).

Table 9-16/G.991.2 – Full Status Request information field

Octet #	Information field	Data type
1	Message ID 12	Message ID

9.5.5.7.13 Status response/SNR – Message ID 139

The performance status/SNR message shall be sent in response to the status request message under the conditions specified in 9.5.5.7.9. The reported integer represents dB SNR noise margin values rounded up. Because each STU only connects to one SHDSL segment, the application interface side SNR margin data shall be 0 (i.e., the network side SNR margin shall be 0 at the STU-C and the customer side SNR shall be 0 at the STU-R).

Table 9-17/G.991.2 – Status response OK/SNR information field

Octet #	Information field	Data type
1	Message ID 139	Message ID
2	Network Side SNR Margin (dB)	Signed char (127 = Not Available)
3	Customer Side SNR Margin (dB)	Signed char (127 = Not Available)
4	Loop ID	Unsigned char (1 = Loop 1, 2 = Loop 2, 3 = Loop 3, 4 = Loop 4)

9.5.5.7.14 SHDSL network side performance status – Message ID 140

This message provides the SHDSL network side performance status. Device fault shall be used to indicate hardware or software problems on the addressed unit. The definition of device fault is vendor dependent but is intended to indicate diagnostic or self-test results. DC continuity fault shall be used to indicate conditions that interfere with span powering such as short and open circuits. The definition of DC continuity fault is vendor dependent.

In octet 11, bits 7..4 are used to indicate that an overflow or reset has occurred in one or more of the modulo counters. Bits 7 and 5 shall indicate that an overflow has occurred since the last SHDSL network side status response. For example, if more than 256 errored seconds occur between SHDSL network side status responses, then the ES modulo counter will overflow. Bits 6 and 4 shall be used to indicate that one or more of the modulo counters have been reset for any reason (e.g., system powerup or a non service-affecting reset.) Bits 7 and 6 shall be cleared to 0 after a SHDSL network side status response is sent to the STU-C. Bits 5 and 4 shall be cleared to 0 after a SHDSL network side status response is sent to the STU-R.

Table 9-18/G.991.2 – SHDSL-network side performance status information field

Octet #	Contents	Data type	Reference
1	Message ID 140	Message ID	
2 bit 7	Reserved		
Bit 6	N – Power Backoff Status	Bit	0 = default 1 = selected
Bit 5	Device Fault	Bit	0 = OK, 1 = Fault
Bit 4	N – DC Continuity Fault	Bit	0 = OK, 1 = Fault
Bit 3	N – SNR Margin alarm	Bit	0 = OK, 1 = alarm
Bit 2	N – Loop Attenuation Alarm	Bit	0 = OK, 1 = alarm
Bit 1	N – SHDSL LOSW Failure Alarm	Bit	0 = OK, 1 = alarm
Bit 0	Reserved		Set to 0
3	N – SHDSL SNR Margin (dB)	Signed char (127 = NA)	
4	N – SHDSL Loop Attenuation (dB)	Signed char (–128 = NA)	
5	N – SHDSL ES Count modulo 256	Unsigned char	
6	N – SHDSL SES Count modulo 256	Unsigned char	
7-8	N – SHDSL CRC Anomaly Count modulo 65536	Unsigned int	
9	N – SHDSL LOSW Defect Second Count modulo 256	Unsigned char	
10	N – SHDSL UAS Count modulo 256	Unsigned char	
11 bit 7	N – Counter Overflow Indication to STU-C		0 = OK 1 = Overflow
11 bit 6	N – Counter Reset Indication to STU-C		0 = OK 1 = Reset
11 bit 5	N – Counter Overflow Indication to STU-R		0 = OK 1 = Overflow
11 bit 4	N – Counter Reset Indication to STU-R		0 = OK 1 = Reset
11 bits 3..0	N-Power Back-Off Base Value (dB)	Unsigned char	0 .. 15
12 bit 7	N-Power Back-Off Extension (dB)	Bit	0→ PBO = Base Value +0 dB 1→ PBO = Base Value +16 dB
12 bits 6..3	Reserved		
12 bits 2..0	Loop ID	Unsigned char	1 = Loop 1 2 = Loop 2 3 = Loop 3 4 = Loop 4

9.5.5.7.15 SHDSL customer side performance status – Message ID 141

This message provides the SHDSL Customer Side Performance Status. Device Fault shall be used to indicate hardware or software problems on the addressed unit. The definition of Device Fault is vendor dependent but is intended to indicate diagnostic or self-test results. DC Continuity Fault shall be used to indicate conditions that interfere with span powering such as short and open circuits. The definition of DC Continuity Fault is vendor dependent.

In octet 11, bits 7..4 are used to indicate that an overflow or reset has occurred in one or more of the modulo counters. Bits 7 and 5 shall indicate that an overflow has occurred since the last SHDSL Customer Side status response. For example, if more than 256 Errored Seconds occur between SHDSL Customer Side status responses, then the ES modulo counter will overflow. Bits 6 and 4 shall be used to indicate that one or more of the modulo counters have been reset for any reason (e.g., system powerup or a non-service-affecting reset). Bits 7 and 6 shall be cleared to 0 after a SHDSL Customer Side status response is sent to the STU-C. Bits 5 and 4 shall be cleared to 0 after a SHDSL Customer Side status response is sent to the STU-R.

Table 9-19/G.991.2 – SHDSL-customer side performance status information field

Octet #	Contents	Data type	Reference
1	Message ID 141	Message ID	
2 bit 7	Reserved		
Bit 6	C – Power Backoff Status	Bit	0 = default 1 = selected
Bit 5	Device Fault	Bit	0 = OK, 1 = Fault
Bit 4	C – DC Continuity Fault	Bit	0 = OK, 1 = Fault
Bit 3	C – SNR Margin alarm	Bit	0 = OK, 1 = alarm
Bit 2	C – Loop Attenuation Alarm	Bit	0 = OK, 1 = alarm
Bit 1	C – SHDSL LOSW Failure Alarm	Bit	0 = OK, 1 = alarm
Bit 0	Reserved		Set to 0
3	C – SHDSL SNR Margin (dB)	Signed char (127 = NA)	
4	C – SHDSL Loop Attenuation (dB)	Signed char (128 = NA)	
5	C – SHDSL ES Count modulo 256	Unsigned char	
6	C – SHDSL SES Count modulo 256	Unsigned char	
7-8	C – SHDSL CRC Anomaly Count modulo 65536	Unsigned int	
9	C – SHDSL LOSW Defect Second Count modulo 256	Unsigned char	
10	C – SHDSL UAS Count modulo 256	Unsigned char	
11 bit 7	C – Counter Overflow Indication to STU-C		0 = OK 1 = Overflow
11 bit 6	C – Counter Reset Indication to STU-C		0 = OK 1 = Reset
11 bit 5	C – Counter Overflow Indication to STU-R		0 = OK 1 = Overflow
11 bit 4	C – Counter Reset Indication to STU-R		0 = OK 1 = Reset

Table 9-19/G.991.2 – SHDSL-customer side performance status information field

Octet #	Contents	Data type	Reference
11 bits 3..0	C-Power Back-Off Base Value (dB)	Unsigned char	0 .. 15
12 bit 7	C-Power Back-Off Extension (dB)	Bit	0→ PBO = Base Value + 0 dB 1→ PBO = Base Value + 16 dB
12 bits 6..3	Reserved		
12 bits 2..0	Loop ID	Unsigned char	1 = Loop 1 2 = Loop 2 3 = Loop 3 4 = Loop 4

9.5.5.7.16 Virtual terminal connect/disconnect request/response (Msg. IDs 6, 7, 134)

Three messages are used to maintain (establish, tear down) virtual terminal sessions between units. A unit may request a connection but must wait for "connect" status response before using the connection. The connection shall remain until a disconnect request is processed or, if implemented, a timeout occurs. At least one session shall be supported by the STU-C. STU-R and SRU may silently ignore the connect request or may respond with a "no connect" status if terminal screens are not supported.

The connect/disconnect process is necessary for handling the case where keyboard messages are received from more than one device. If a unit cannot accommodate another connect request, it shall send the "no connect" response.

The connect request message can be sent to cause a refresh of the current screen. When a connect request is accepted the "connect" response shall be transmitted, followed by screen messages with the current screen. If this is a new connection then the first screen shall be sent. The end unit that issues the connect request (Message 6) shall issue the corresponding request (Message 7) to terminate the virtual terminal session. A far-end unit shall respond with Virtual Terminal "no connect" status (Message 134) when it receives a keyboard message from the near-end unit that terminates a virtual terminal session. (This lets the near-end know that the far-end has terminated the connection.) If the far-end unit has dropped the terminal session and a keyboard message is received, the far-end unit shall respond with Message 134 – "no connect".

For any keyboard character that has special meaning at the near-end (e.g., and escape command), means shall be provided to send that keyboard character to the far end. (This is analogous to the CTRL-] escape command used in TELNET sessions. When one has escaped in a TELNET session to the local terminal, one can typically issue a "send escape" command or similar to send the CTRL-] character to the far end.)

Table 9-20/G.991.2 – Virtual terminal connect

Octet #	Contents	Data type	Reference
1	Message ID 6 – Virtual Terminal Connect	Message ID	

Table 9-21/G.991.2 – Virtual terminal disconnect

Octet #	Contents	Data type	Reference
1	Message ID 7 – Virtual Terminal Disconnect	Message ID	

Table 9-22/G.991.2 – Virtual terminal connect response

Octet #	Contents	Data type	Reference
1	Message ID 134 – Virtual Terminal Connect Response	Message ID	
2	Connection status		1 = connected 0 = no connect

9.5.5.7.17 Screen message/keyboard message (Msg. IDs 8, 136)

Keyboard and screen messages are only sent over an active connection between units. Keyboard messages shall be 1 to 8 data octets per message. Queuing of keystrokes from the customer may affect user response times and should be done with care. Screen messages shall be 1 to 24 data octets per message, and their contents are vendor defined. See 9.5.6 for more information on Screen/Keyboard messages.

Table 9-23/G.991.2 – Keyboard information field

Octet #	Contents	Data type	Reference
1	Message ID 8 – Keyboard	Message ID	
2.. (L + 1)	ASCII character(s) and escape sequences	char array	

Table 9-24/G.991.2 – Screen information field

Octet #	Contents	Data type	Reference
1	Message ID 136 – Screen	Message ID	
2.. (L + 1)	ASCII characters and escape sequences	char array	

9.5.5.7.18 Maintenance Request – System Loopback Messages (9)

The Maintenance Request – System Loopback Message contains loopback commands for all of the elements on the span. The contents of the Maintenance Request – System Loopback message are shown in Table 9-25. The System Loopback message shall have a broadcast destination address when sent from the STU-C. When optionally sent from the STU-R, the System Loopback message shall have the STU-C as its destination address. Upon reception of this message, each SRU and STU shall comply with its corresponding command field and respond to the sender with the Maintenance Status message. Note that the SRUs are numbered consecutively beginning with closest SRU to the STU-C. Each SRU shall determine its number by subtracting 2 from its network side EOC address. Since the network side EOC addresses must be known, the STU-R shall not use the System Loopback Message if the STU-C is offline. To invoke SRU loopbacks while the STU-C is offline, the STU-R shall use the Maintenance Request-Element Loopback message. (Maintenance request messages may also be used by the STU devices to poll for current loopback status, using the unchanged bit flags.)

Table 9-25/G.991.2 – Maintenance Request – System Loopback information field

Octet #	Contents	Data type	Reference
1	Message ID 9 – Maintenance Request-System Loopback		
2	STU-C Loopback Commands	Bit flags	Table 9-26
3	STU-R Loopback Commands	Bit flags	Table 9-26
4	SRU #1 Loopback Commands	Bit flags	Table 9-26
5	SRU #2 Loopback Commands	Bit flags	Table 9-26
6	SRU #3 Loopback Commands	Bit flags	Table 9-26
7	SRU #4 Loopback Commands	Bit flags	Table 9-26
8	SRU #5 Loopback Commands	Bit flags	Table 9-26
9	SRU #6 Loopback Commands	Bit flags	Table 9-26
10	SRU #7 Loopback Commands	Bit flags	Table 9-26
11	SRU #8 Loopback Commands	Bit flags	Table 9-26

Table 9-26/G.991.2 – Loopback command bit flag definitions

Bit positions	Definition
7	Reserved
6	Clear All Maintenance States (including any proprietary states)
5	Initiate Special Loopback
4	Terminate Special Loopback
3	Initiate Loopback toward the Network
2	Initiate Loopback toward the Customer
1	Terminate Loopback toward the Network
0	Terminate Loopback toward the Customer
NOTE – Bit set to 1 – perform action, Bit Set to 0 – no action taken, report current status.	

9.5.5.7.19 Maintenance Request – Element Loopback Message ID 10

The Maintenance Request – Element Loopback Message contains loopback commands for an individual element. The contents of the Maintenance Request – Element Loopback message are shown in Table 9-27. The Element Loopback message shall have an individual unit's destination address according to the data flow addresses described in 9.5.2. Upon reception of the Element Loopback message, the addressed unit shall comply with the loopback commands and reply with the Maintenance Status Response message.

Table 9-27/G.991.2 – Maintenance Request – Element Loopback information field

Octet #	Contents	Data type	Reference
1	Message ID 10 – Maintenance Request	Message ID	
2	Loopback Commands	Bit flags	Table 9-26

9.5.5.7.20 Maintenance Status Response Message ID 137

Maintenance status is sent in response to the Maintenance Request – System Loopback, Maintenance Request – Element Loopback, Status Request, and Full Status Request query messages. The "Special loopback" is defined for the STU-R as a Maintenance Termination Unit (MTU) loopback; it is not defined at other units.

Table 9-28/G.991.2 – Maintenance Status information field

Octet #	Contents	Data type	Reference
1	Message ID 137 – Maintenance Status-Loopback	Message ID	
2 bit 7	Loopback Timeout Status	Bit	0 = unchanged, 1 = changed
2 bit 6	Proprietary Maintenance State active	Bit	0 = off, 1 = on
2 bit 5	Special loopback active	Bit	0 = off, 1 = on
2 bit 4	Loopback active toward STU-R	Bit	0 = off, 1 = on
2 bit 3	Loopback active toward STU-C	Bit	0 = off, 1 = on
2 bit 2	Local or span-powered unit	Bit	0 = span powered 1 = local powered
2 bit 1	Customer Tip/Ring Reversal	Bit	0 = normal 1 = reversed
2 bit 0	Network Tip/Ring Reversal	Bit	0 = normal 1 = reversed

9.5.5.7.21 Soft restart/power backoff disable Message ID 15

The purpose of this message is to switch a receiver between the default and selected modes of power backoff. If default mode is set, PBO shall be set to the default value. Otherwise, in selected mode, PBO may be negotiated through G.994.1 to another value. In order for a change in power backoff mode to take effect, the receiver must reactivate. The Soft Restart request shall cause the receiving unit to terminate the corresponding SHDSL connection and enter the Exception State (Figure 6-7). The connection shall not be terminated unless the corresponding Soft Restart bit is set in this message. The receiving unit shall wait 5 ± 1 s before terminating the SHDSL connection.

This message carries the command to set the power backoff mode. The power backoff mode received in this message shall be maintained as long as power is applied to the unit. Maintaining the power backoff mode in non-volatile storage is optional. Note that the configuration of power backoff mode applies to the receiver; i.e., the receiver requests a PSD mask based on both the received power and the configuration of its power backoff mode.

Table 9-29/G.991.2 – Soft restart information field

Octet #	Contents	Data type	Reference
1	Message ID 15 – Soft Restart/Backoff	Message ID	
2 bits 7..2	Reserved		
2 bit 1	Network Side Power Backoff Setting	Bit	0 = default 1 = selected
2 bit 0	Network Side Soft Restart (after 5 s)	Bit	0 = no Restart 1 = Restart
3 bits 7..2	Reserved		
3 bit 1	Customer Side Power Backoff Setting	Bit	0 = default 1 = selected
3 bit 0	Customer Side Soft Restart (after 5 s)	Bit	0 = no Restart 1 = Restart

9.5.5.7.22 Segment management message – (IDs 64-88, 192-216)

A range of Message IDs is reserved for segment management (e.g., continuous precoder update).

9.5.5.7.23 Proprietary messages (IDs 112-119, 240-247)

A range of Message IDs is reserved for proprietary messages. It is the responsibility of the STU to address Proprietary Messages to the appropriate destination. An SRU shall either process or forward a proprietary message. A proprietary message shall not be broadcast.

9.5.5.7.24 Proprietary external message (ID 120)

Support for external data ports is optional. No interface for an external data port is specified in this Recommendation. If an STU does not have an external data port, then it shall ignore any received Proprietary External Messages.

Table 9-30/G.991.2 – External information field

Octet #	Contents	Data type	Reference
1	Message ID 120 – External	Message ID	
2	Logical Port Number	Unsigned char	
3.. (*N* + 2)	External message data (*N* octets)		

9.5.5.7.25 G.997.1 external message (ID 121)

Support for G.997.1 [3] external messaging is optional. The interface for G.997.1 messages is beyond the scope of this Recommendation. If an STU does not have an interface for G.997.1 messaging, it shall ignore any received G.997.1 External Messages.

Logical port number FF_{16} is reserved for indicating the transport of SNMP packets, as described in 6.4/G.997.1. SNMP packets may be transmitted using one or more such messages.

Table 9-31/G.991.2 – G.997.1 external information field

Octet #	Contents	Data type	Reference
1	Message ID 121	Message ID	
2	Logical Port Number	Unsigned char	
3.. (*N* + 2)	G.997.1 External message data (*N* octets)		

9.5.5.7.26 Generic Unable to Comply (UTC) Message (ID 144)

The Generic UTC message should be sent back to the source unit in the event that the destination unit is unable to comply with the request. In this case, the definition of UTC is vendor dependent. Note that this message is not meant to replace the UTC bit in those response messages that contain a UTC bit.

Table 9-32/G.991.2 – Generic Unable to Comply (UTC) information field

Octet #	Contents	Data type	Reference
1	Message ID 144 – Generic UTC	Message ID	
2	Message ID of request message	Unsigned char	

9.5.5.7.27 Mapping Request – Message ID 23

The Mapping Request Message is used to determine the mapping between the physical pair (or loop) number labelled on the equipment and the logical wire pair (or loop) ordinal number (7.2.1.5). While this mapping is vendor specific, this information is useful for troubleshooting circuits. The response to this request shall be message ID 151.

Table 9-32a/G.991.2 – Mapping Request information field

Octet #	Contents	Data type	Reference
1	23	Message ID	

9.5.5.7.28 Mapping Response – Message ID 151

The Mapping Response Message is sent in response to a Mapping Request Message (message ID 23). It is used to determine the mapping between the physical pair (or loop) number and the logical wire pair (or loop) ordinal number. The physical pair number is the number labelled externally on the equipment. The logical wire pair number is determined from bits 4145 to 4146 of the activation frame from the STU-R device as specified in 7.2.1.5. The physical pair number is composed of two octets, with the first octet containing the most significant byte, and the second octet containing the least significant byte. For example, if the 16-bit number in octets 3/4 contains the value 4, then logical wire pair 1 from 7.2.1.5 is transported over the equipment's physical pair labelled number 4. If the responding unit is a repeater, then the mapping response information for the network side of the repeater will be sent first with bit 3 of octet two set to zero, followed immediately by the mapping response information for the customer side of the repeater with bit 3 of octet two set to one.

Table 9-32b/G.991.2 – Mapping Response information field

Octet #	Contents	Data type	Reference
1	151	Message ID	
2 bit 7	Response Side	Bit	0 = network side information 1 = customer side information
2 bits 6-3	Reserved		
2 bits 2-0	Number of Wire Pairs, *M*	Unsigned	1 = 1 pair 2 = 2 pair 3 = 3 pair 4 = 4 pair
3-4	Physical Pair Number Corresponding to Logical Wire Pair 1 (7.2.1.5)	Unsigned Char	
5-6	Physical Pair Number Corresponding to Logical Wire Pair 2 (7.2.1.5)	Unsigned Char	
	. . .	. . .	
$2 \times M + 1$ – $2 \times M + 2$	Physical Pair Number Corresponding to Logical Wire Pair *M* (7.2.1.5)	Unsigned Char	

9.5.6 Examples of virtual terminal control functions

This informative note gives examples of some common ANSI X3.4-1986 (R1997) [B3] escape sequences.

Table 9-33/G.991.2 – Examples of ANSI X3.4-1986 (R1997) control functions

Description	Format	Comments
Erase entire screen (ED)	ESC [2 J	
Position cursor (CUP)	ESC [RR;CCH	(Note)
Position cursor (in column 1)	ESC [RRH	Subset of Position cursor
Home cursor	ESC [H	Subset of Position cursor
NOTE – ESC has the value of $1B_{16}$. RR is the row number; CC is the column number expressed as ASCII digits. As an example, row 4 column 12 would encode as ESC [4;12H. The hexadecimal equivalent of this sequence is $1B_{16}$ $5B_{16}$ 34_{16} $3B_{16}$ 31_{16} 32_{16} 48_{16}. The screen starts with row 1, column 1.		

10 Clock architecture

10.1 Reference clock architecture

Due to the multiple applications and variable bit rates called for in SHDSL, a flexible clocking architecture is required. The STU-C and STU-R symbol clocks are described in terms of their allowed synchronization references.

The SHDSL reference configuration permits the flexibility to provide a symbol clock reference based on the sources shown in Figure 10-1. It illustrates the clock reference options in the context of a simplified SHDSL reference model. Table 10-1 lists the normative synchronization configurations as well as example applications.

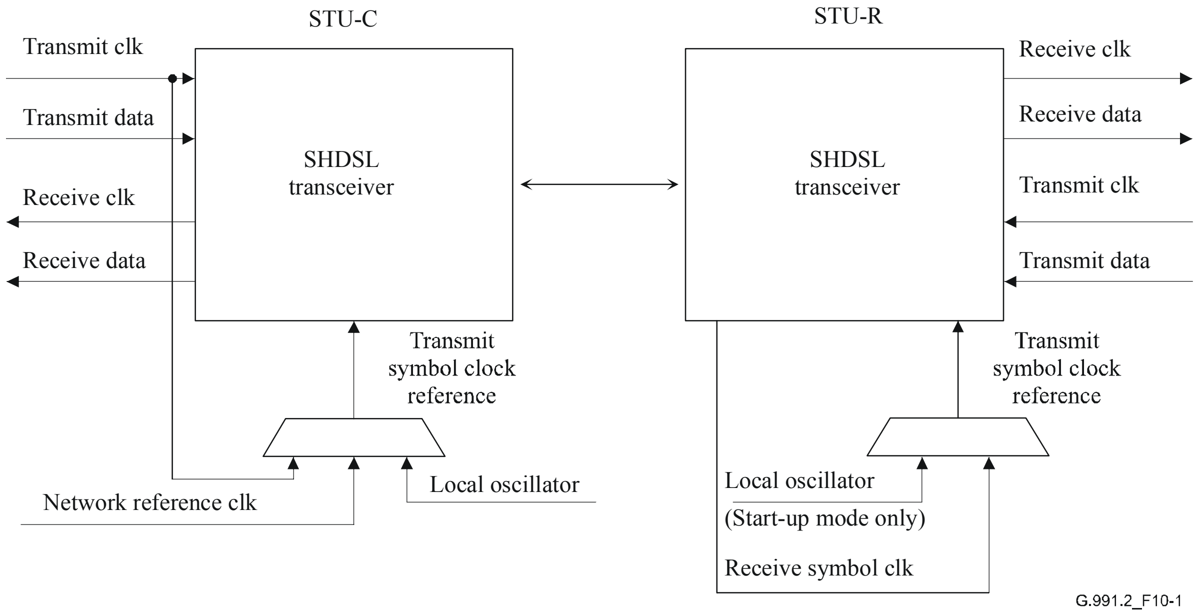


Figure 10-1/G.991.2 – Reference clock architecture

Table 10-1/G.991.2 – Clock synchronization configurations

Mode number	STU-C symbol clock reference	STU-R symbol clock reference	Example application	Mode
1	Local oscillator	Received symbol clock	"Classic" HDSL	Plesiochronous
2	Network reference clock	Received symbol clock	"Classic" HDSL with embedded timing reference	Plesiochronous with timing reference
3a	Transmit data clock or network reference clock	Received symbol clock	Main application is synchronous transport in both directions	Synchronous
3b	Transmit data clock	Received symbol clock	Synchronous downstream transport and bit-stuffed upstream is possible	Hybrid: downstream: synchronous upstream: plesiochronous

10.2 Clock accuracy

At all rates, the transmit symbol clock during data mode from any SHDSL device shall be accurate to within ±32 ppm of the nominal frequency. During activation, the STU-C shall maintain ±32 ppm accuracy of its transmit symbol clock, but the STU-R transmit symbol clock may vary up to ±100 ppm.

10.3 Definitions of clock sources

The following definitions shall apply to the clock sources shown in Figure 10-1.

10.3.1 Transmit symbol clock reference

A reference clock from which the actual transmit symbol clock is derived (i.e., the STU's transmit symbol clock is synchronized to this reference).

10.3.2 Local oscillator

A clock derived from an independent local crystal oscillator.

10.3.3 Network reference clock

A primary reference clock derived from the network.

10.3.4 Transmit data clock

A clock that is synchronous with the transmitted data at the application interface.

10.3.5 Receive symbol clock

A clock that is synchronous with the downstream received symbols at the SHDSL line interface. This clock is used as the transmit symbol clock reference in the STU-R.

10.3.6 Receive clock

A clock that is synchronous with the received data at the application interface.

10.4 Synchronization to clock sources

In synchronous mode, the STU-C can be synchronized to the transmit data clock or to a network reference clock. If a network reference clock is used, the transmit data clock must be synchronized to the network reference clock. (The various transmit data rates are independent of the reference clock frequency.)

When available, the network reference clock shall be either a fundamental 8 kHz network clock or a related reference clock at some multiple of 8 kHz. Such reference clocks are typically 1544 MHz or 2048 MHz, although in some applications other frequencies, such as 64 kHz, may be available. These related clocks include implicit 8 kHz[1] timing signals. Selection of a specific network clock reference frequency shall be application dependent.

11 Electrical characteristics

This clause specifies conformance tests for SHDSL equipment. These out-of-service tests verify the electrical characteristics of SHDSL metallic interfaces.

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[1] The 6 ms SHDSL frame for synchronous data transport and the network 8 kHz clock have a fixed relationship. Each SHDSL frame contains $48(1 + i + n \times 8)$ bits ($i = 0 \ldots 7$ and $n = 3 \ldots 36$, or, optionally, $n = 37 \ldots 89$, as described in Annex F). The relationship can be calculated with: T = 6 ms/48 = 125 µs and f = 1/T = 8 kHz. At the STU-R, an 8 kHz clock signal can be derived from the synchronous 6 ms frame.

11.1 Longitudinal balance

Longitudinal balance or longitudinal conversion loss (LCL) is a figure of merit describing the coupling between longitudinal V_L (common mode) and metallic V_M (normal mode) signal components. This term is equivalent to the familiar common mode rejection ratio (CMRR) and defined as follows:

$$\text{Longitudinal Balance (dB)} = 20\log\left|\frac{V_L}{V_M}\right|$$

Longitudinal balance at the SHDSL loop interface shall be measured with a coupling circuit having a metallic termination of 135 Ω and a longitudinal termination of 33.8 Ω (Figure 11-1). Example coupling circuits are shown in Appendix I. This test shall be performed with the DUT transmitter turned off (quiet mode) and with span power circuitry (in either CO and RT units) activated by an appropriate external DC current source/sink. The active power feed requirement may be waived for locally powered systems.

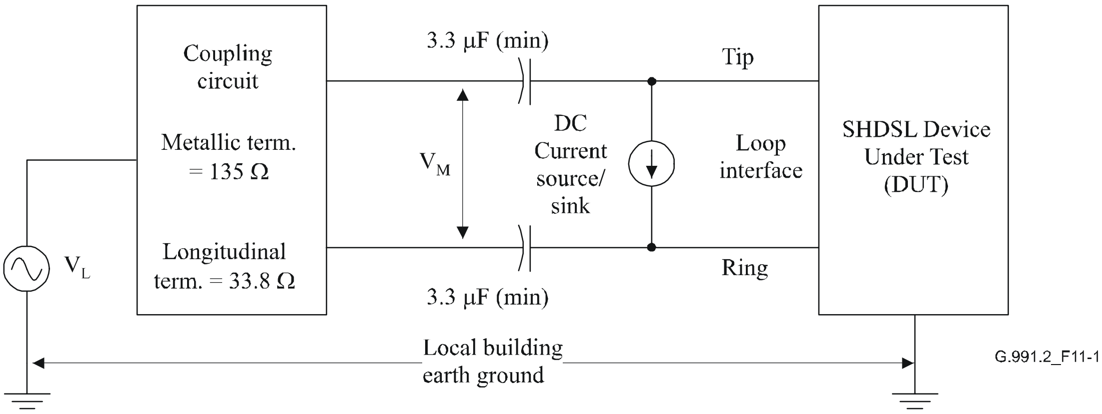


Figure 11-1/G.991.2 – Longitudinal balance measurement

The measured longitudinal balance at the SHDSL loop interface shall lie above the specified limit mask defined in Figure 11-2. The values of the parameters in the figure are region-specific and are specified in A.5.4 and B.5.4. The longitudinal test circuit shall be calibrated such that when a 135 Ω resistor (placed across tip and ring) is substituted for the device under test and the DC current source/sink is disconnected, the measured longitudinal balance shall be at least 20 dB above the limit mask. The longitudinal balance shall be measured over the frequency range of 20 kHz to 2 MHz.

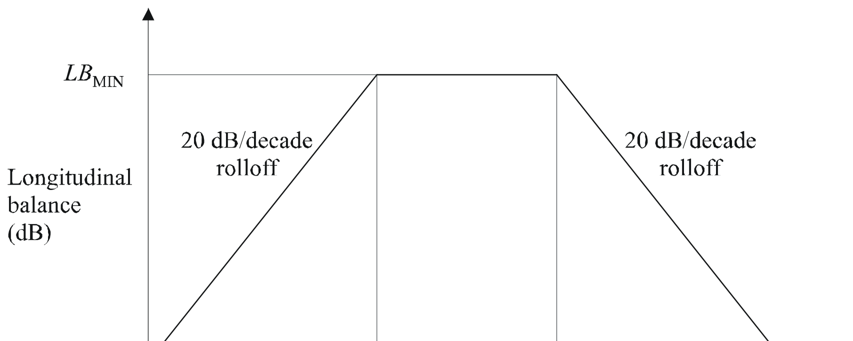


Figure 11-2/G.991.2 – Longitudinal balance limit mask

11.2 Longitudinal output voltage

Longitudinal output voltage at the SHDSL loop interface shall be measured with a coupling circuit having a metallic termination of 135 Ω and a longitudinal termination of 33.8 Ω as shown in Figure 11-3. Example coupling circuits are shown in Appendix I. This test shall be performed with the transmitter active (sending random data) and the span power circuitry (in either CO and RT units) activated by an appropriate external DC current source/sink. The active power feed requirement may be waived for locally powered systems.

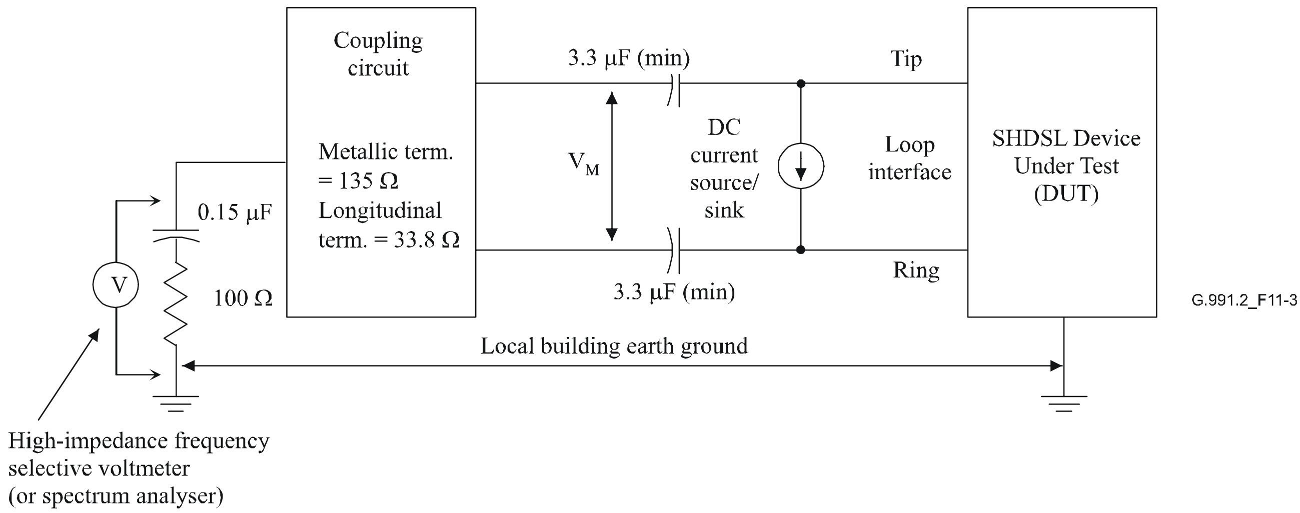


Figure 11-3/G.991.2 – Longitudinal output voltage measurement

The measured longitudinal output rms voltage at the SHDSL loop interface shall be less than –50 dBV over any 4 kHz frequency band when averaged over one second periods. The measurement frequency range is region-specific and is specified in A.5.5 and B.5.5.

11.3 Return loss

This test measures return loss at the SHDSL loop interface with respect to a 135 Ω reference (line) impedance. In SHDSL applications, return loss is generally used as a measure of termination impedance distortion (deviation in both magnitude and phase from the reference impedance value). Return loss limits are necessary to prevent large termination mismatches between equipment from compliant vendors. Return loss may be measured directly using an impedance analyser or indirectly as a voltage output in a bridge circuit. For either method, care must be taken to prevent measurement errors from possible unintentional circuit paths between the common ground of the measuring instrument(s) and the DUT power feed circuitry. In addition, when measuring under span powered conditions, the test instrument must be galvanically isolated from the loop interface to prevent damaging the test equipment with the high voltage DC power feed. For measurements performed with an impedance analyser return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{Z_{TEST}(f)+Z_{REF}}{Z_{TEST}(f)-Z_{REF}}\right|$$

where:

$Z_{TEST}(f)$ measured complex impedance at frequency f at the DUT loop interface

Z_{REF} reference impedance (135 Ω).

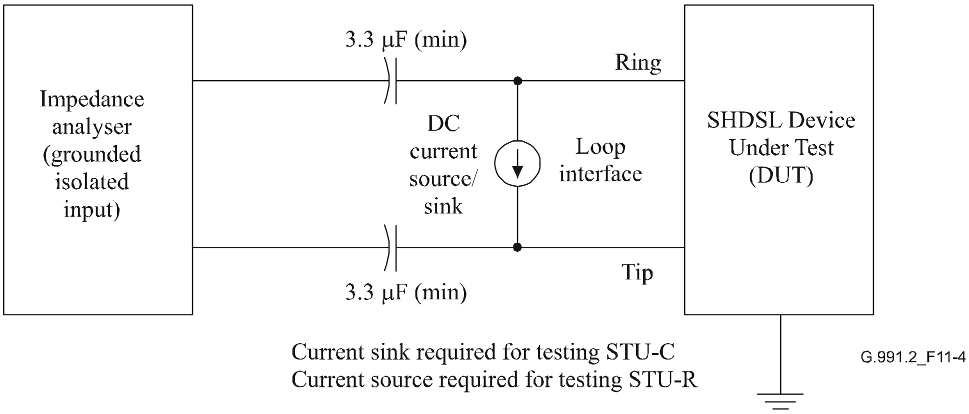


Figure 11-4/G.991.2 – Return loss impedance analyser test method

For measurements performed with a test bridge the return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{V_{IN}(f)}{V_{OUT}(f)}\right|$$

An example return loss test bridge is shown in Appendix I.

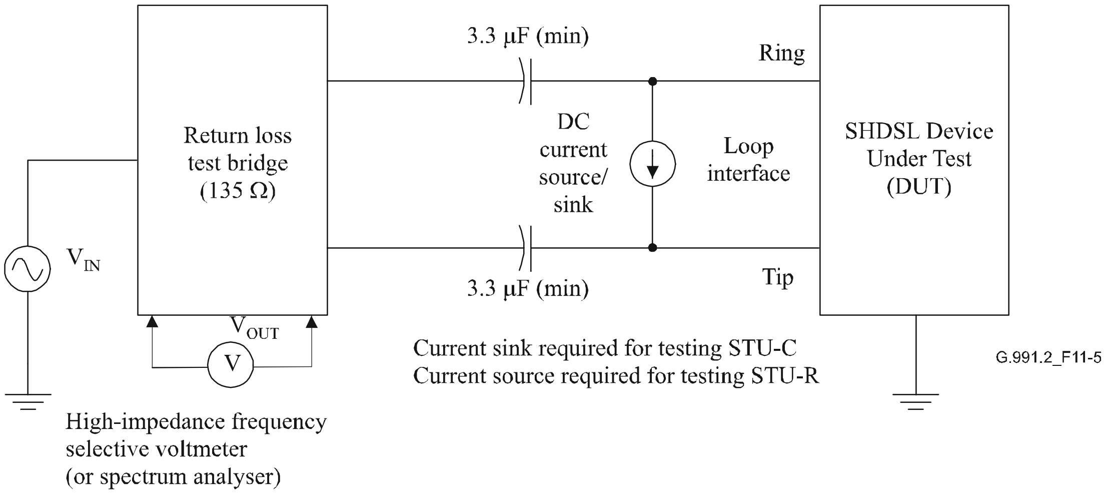


Figure 11-5/G.991.2 – Return loss bridge test method

The return loss test shall be performed with the DUT transmitter turned off (quiet mode). The DUT may be tested span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R, the test shall be performed with power (DC voltage) applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance. Note that the DC current source/sink must present a high impedance (at signal frequencies) to common ground.

The nominal driving point impedance of the SHDSL loop interface shall be 135 Ω. Return loss shall be measured with either the impedance analyser method of Figure 11-4 or the bridge method of Figure 11-5. The measured return loss values relative to 135 Ω shall lie above the limit mask specified in Figure 11-6. The values of the parameters are region-specific, and are specified in A.5.2 and B.5.2. The loop interface return loss shall be measured over the frequency range of 1 kHz to 2 MHz.

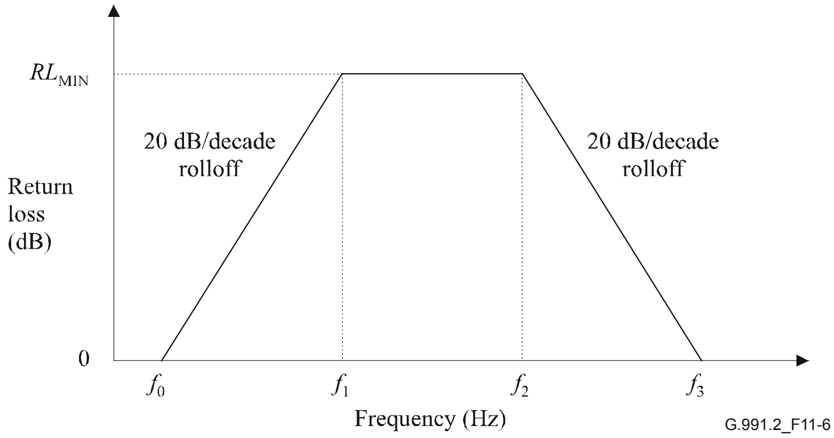


Figure 11-6/G.991.2 – Return loss limit mask

11.4 Transmit power testing

The total average transmit power may be tested while span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R, the test shall be performed with power (DC voltage) applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance. The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Note that the DC current source/sink must present a high impedance (at signal frequencies) to common ground.

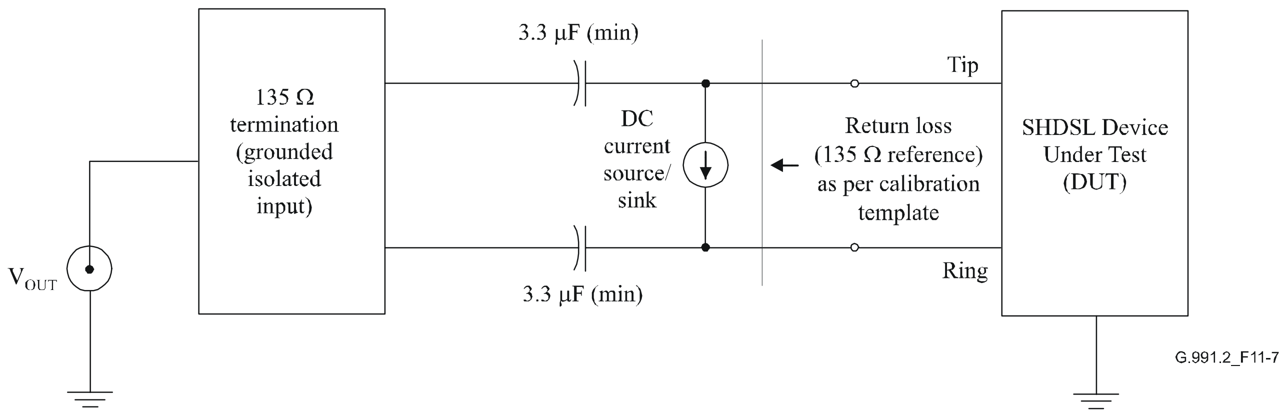


Figure 11-7/G.991.2 – PSD/total power measurement set-up

11.4.1 Test circuit

The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. When the driving point impedance of the test circuit meets the calibration requirements defined in 11.4.2, the test circuit will not introduce more than ±0.25 dB error with respect to a perfect 135 Ω test load. An example test circuit is shown in Appendix I. Note that the same circuit may be used for measuring total transmit power and transmit PSD.

11.4.2 Test circuit calibration

The nominal driving point impedance of the test circuit shall be 135 Ω. The minimum return loss with respect to 135 Ω over the frequency band of 3 kHz to 3 MHz shall be 35 dB from 10 kHz to 500 kHz with a slope of 20 dB/decade below and above these corner frequencies.

NOTE – 35 dB return loss will allow ±0.20 dB measurement error with respect to the nominal 135 Ω value.

11.4.3 Total transmit power requirement

The average transmit power of the STU-C shall be measured while continuously sending either signal S_c (6.2.2.2) or signal $Data_c$ (6.2.2.7). If $Data_c$ is used, the total power measured into 135 Ω shall fall in the range (P_{SHDSL} ± 0.5 dB) as specified in A.4 and B.4. If S_c is used, the total power measured into 135 Ω shall fall in the range (P_{SHDSL} – 0.2 dB ± 0.5 dB). The average transmit power of the STU-R shall be measured while continuously sending either signal S_r (6.2.2.3) or signal $Data_r$ (6.2.2.7). If $Data_r$ is used, the total power measured into 135 Ω shall fall in the range (P_{SHDSL} ± 0.5 dB) as specified in A.4 and B.4. If S_r is used, the total power measured into 135 Ω shall fall in the range (P_{SHDSL} – 0.2 dB ± 0.5 dB). This power measurement in activation mode will be 0.2 dB lower than the associated data mode transmit power due to the 2-PAM constellation definition.

The transmit power spectral density of the STU-C shall be measured while continuously sending either signal S_c (6.2.2.2) or signal $Data_c$ (6.2.2.7). The transmit power spectral density of the STU-R shall be measured while continuously sending either signal S_r (6.2.2.3) or signal $Data_r$ (6.2.2.7). If $Data_c$ or $Data_r$ is used, the measured transmit PSD into 135 Ω shall remain below the corresponding *PSDMask*(f) from A.4 and B.4. If S_c or S_r is used, the measured transmit PSD into 135 Ω shall remain below the corresponding *PSDMask*(f) from A.4 and B.4 reduced by 0.2 dB in the passband (i.e., *PSDMask*(f) with PBO increased by 0.2 dB).

11.4.3.1 Transmit power spectral density test procedure

The transmit power spectral density (PSD) may be tested span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R, the test shall be performed with power (DC voltage) applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance.

The transmit power spectral density for the STU-C and STU-R shall be measured with signals as defined in 11.4.3. The transmit power spectral density shall be measured over the frequency range of 1 kHz to 3 MHz. The STU-C transmit signal shall be compliant with the appropriate A.4 or B.4 PSD requirements. The STU-R transmit signal shall be compliant with the appropriate A.4 or B.4 PSD requirements.

11.4.3.2 PSD test circuit and calibration

The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. The test circuit shall meet the requirements of 11.4.2.

11.5 Signal transfer delay

The STU shall be capable of providing PMD-layer one-way, single-span latency of 500 µs or less for user data rates of 1.5 Mbit/s and above, and 1.25 ms or less for user data rates below 1.5 Mbit/s as measured between the α and ß interfaces.

12 Conformance testing

12.1 Micro-interruptions

A micro-interruption is a temporary interruption due to external mechanical action on the copper wires constituting the transmission segment, for example, at a cable splice. Splices can be hand-made wire-to-wire junctions, and during cable life oxidation phenomena and mechanical vibrations can induce micro-interruptions at these critical points. Example causes of this impairment include a large motor vehicle driving over a buried cable installation or an aerial cable movement from wind forces.

The effect of a micro-interruption on the transmission system can be a failure of the digital transmission link, together with a failure of the span power feeding (if provided) for the duration of the micro-interruption. The operating objective is that in the presence of a micro-interruption of specified maximum length the system shall not reset, and the system shall automatically reactivate with a complete start-up procedure if a reset occurs due to an interruption.

The configuration for micro-interruption susceptibility testing is shown in Figure 12-1. In this arrangement, a periodic trigger signal *S* stimulates a normally closed micro-relay device inducing periodic micro-interruptions on the transmission link. Note that the micro-interruptions are induced on one termination at a time. The test loops shall be composed of 1.5 km of 0.4 mm (or 5000' of 26 AWG) copper wire, and the tests shall be conducted at the maximum supported data rate. Using the test arrangement as described in Figure 12-1 with local powering on, the SHDSL transceivers shall not be reset by a micro-interruption of at least t = 10 ms when stimulated with a signal of period T = 5 s for a test interval of 60 s at a single termination. The micro-interruptions shall be induced at both the STU-C and STU-R terminations. This test shall be repeated with span-powering on and a micro-interruption of at least t = 1 ms.

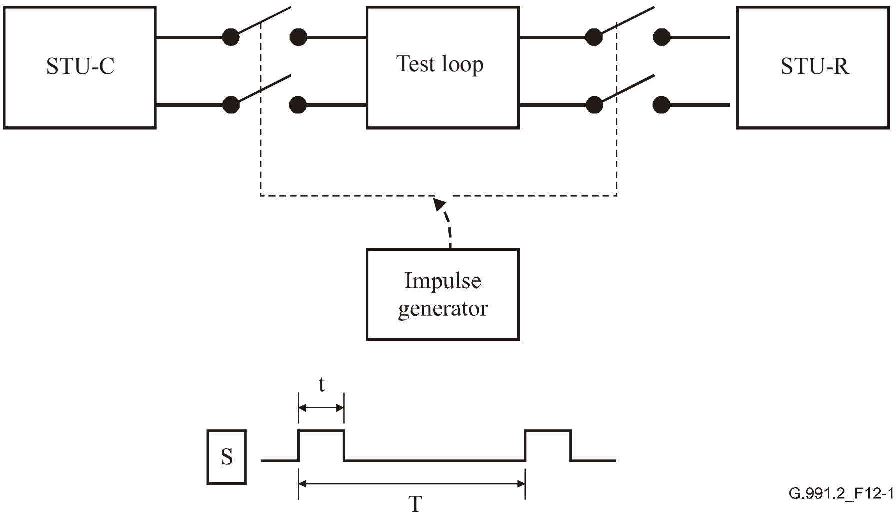


Figure 12-1/G.991.2 – Micro-interruption test circuit

Annex A

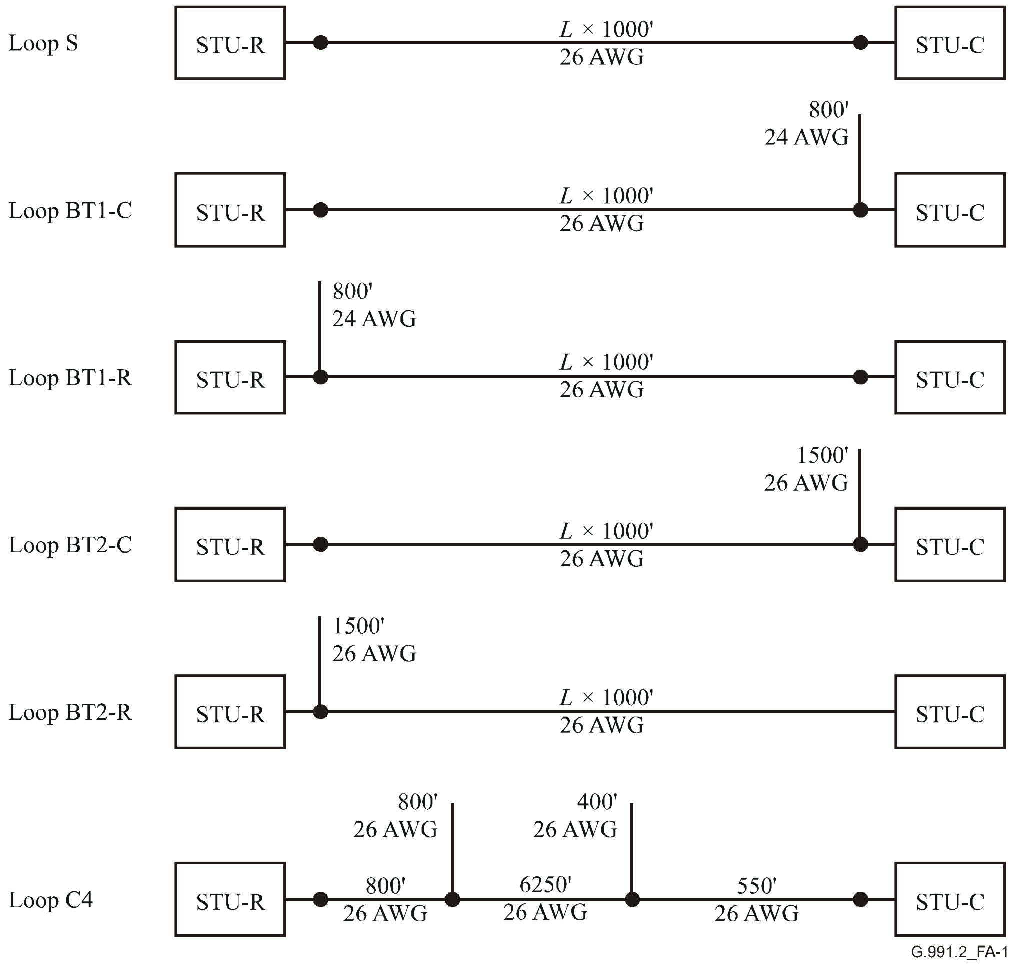
Regional requirements – Region 1

A.1 Scope

This annex describes those specifications that are unique to SHDSL systems operating under conditions such as those typically encountered within the North American network. The clauses in this annex provide the additions and modifications to the corresponding clauses in the main body.

A.2 Test loops

The primary constants for the following test loops are listed in Annex A/G.996.1 [6]. Note that the test loops shown in Figure A.1 are PIC and specified at 70° F (21.1° C). Loop 0 is the null loop: ≤ 10' and ≤ 26 AWG.



NOTE – AWG = American Wire Gauge; 26 AWG = 0.4 mm, 24 AWG = 0.5 mm.
Distances in feet ('): 1000' = 0.3048 km.

Figure A.1/G.991.2 – Test loops

A.3 Performance Tests

This clause specifies performance tests for SHDSL equipment. These out-of-service tests verify the performance of SHDSL in impaired environments.

Figure A.2 shows the test set-up for measuring the performance of SHDSL systems in the presence of noise impairments. The test system consists of an SHDSL central office transceiver (STU-C) and a remote end transceiver (STU-R). The SHDSL transceivers are connected by a test loop. Simulated noise is locally injected into the test loop through the specified coupling circuit at the receiving transceiver.

Bit error ratio (BER) measurement is performed by applying a pseudo-random binary sequence (PRBS) test signal at one transceiver input and detecting errors in the received PRBS data stream of the other transceiver. The PRBS signal shall have a minimum period of $2^{23} - 1$. BER measurement shall be performed for both directions of transmission and the tests in each direction shall be performed in full-duplex mode with both SHDSL transceivers simultaneously transmitting data. In all cases these noise impairment tests shall be performed one unit at a time (i.e., the STU-C and STU-R are not impaired simultaneously) and with noise from only one impairment source active at a time.

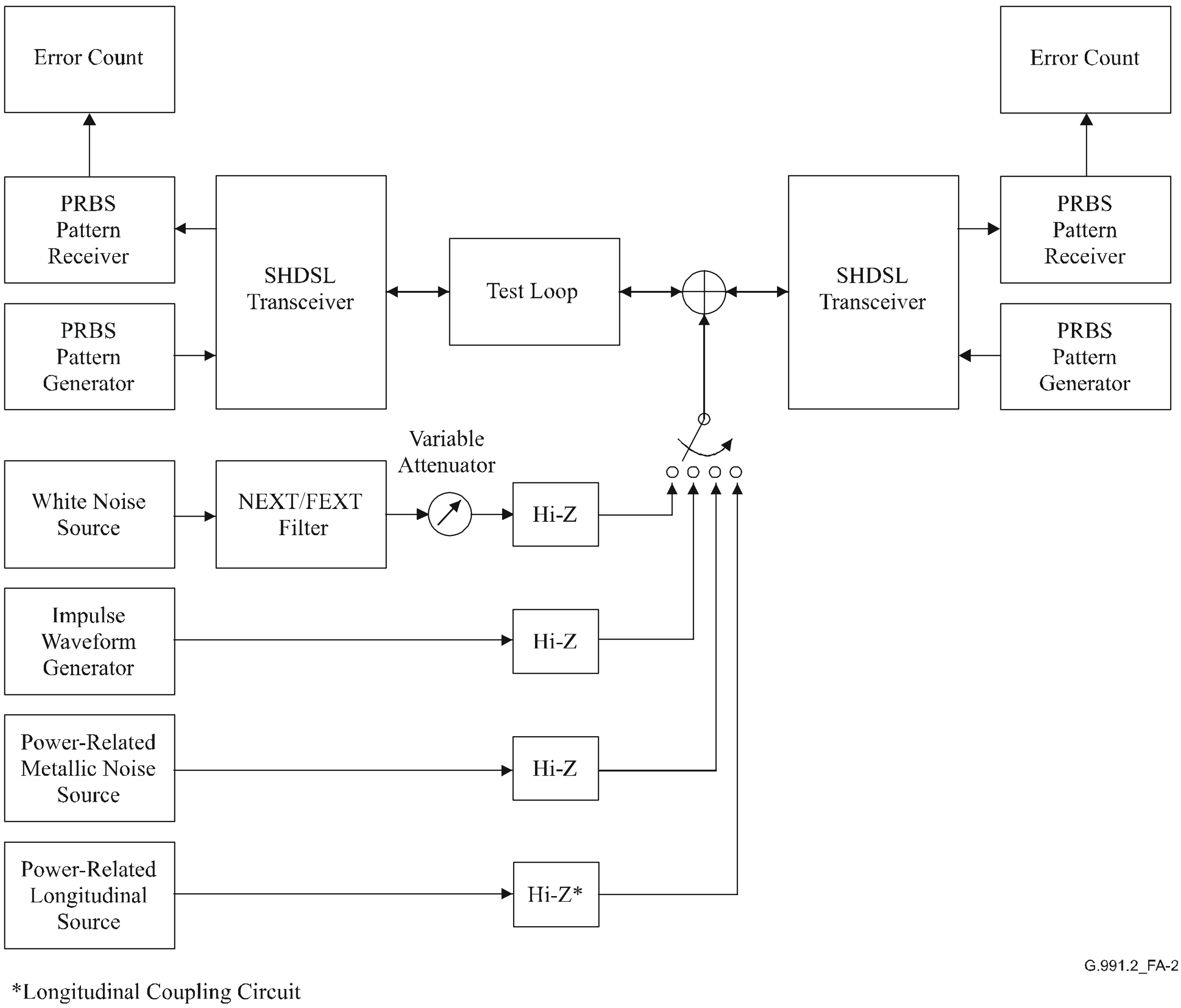


Figure A.2/G.991.2 – Crosstalk margin and impulse noise test set-up

A.3.1 Crosstalk margin tests

A.3.1.1 Crosstalk noise injection

Simulated crosstalk (NEXT and FEXT) is introduced by injecting a calibrated, filtered Gaussian noise source into the test circuit. The crosstalk shall be locally injected into the test loop at the receiving transceiver through a balanced high-impedance parallel-connected feed network. The high-impedance parallel-connected feed network allows injection of the desired crosstalk power level without disturbing the transmission characteristics or driving point impedance of the test loop. The injection circuit shall have a Thevenin output impedance of at least 4 kΩ. An example crosstalk signal injection circuit is shown in Figure I.1.

A.3.1.2 Calibration accuracy of crosstalk generator

The simulated crosstalk shall have the total power and the power spectral density (PSD) defined in A.3.3. However, if the method of generating simulated crosstalk is as defined in Figure A.2, then the power level and PSD accuracy will depend on the accuracy of the filters designed to shape the white noise for each injected crosstalk source. The highest level of accuracy is required within the frequency band (or bands) corresponding to the largest values of the PSD for each crosstalk source.

For each specified crosstalk source, the accuracy of the simulated PSD obtained shall be ±1.0 dB within the ideal PSD template (defined by the equations in A.3.3) over the frequency band(s) where the ideal PSD template is within 30 dB of its maximum value. The measured average power (integral of the crosstalk PSD function) for each specified crosstalk source shall be within ±0.25 dB of the integrated power of the ideal specified crosstalk PSD template (A.3.3).

The white noise source of Figure A.2 shall cover the frequency band from DC to 1.5 MHz and have a Gaussian amplitude distribution with a crest factor of at least 5.0.

A.3.1.3 Calibration measurement of crosstalk generator

The PSD and average power for each crosstalk test scenario shall be calibrated by measuring the output of the crosstalk injection circuit with the test loop replaced by a load of two parallel 135 Ω resistors (67.5 Ω) and no connected terminal equipment. The two parallel 135 Ω resistors simulate the terminating load of a zero-length loop. The crosstalk signal shall be measured as a voltage by a high-impedance frequency-selective voltmeter (i.e., spectrum analyser) and converted into a power level assuming a 135 Ω reference impedance. This procedure effectively measures the crosstalk power fed into a single resistor (one side of the loop only). The measured crosstalk PSD(s) and average crosstalk power(s) coupled into the calibration load must remain within the limits defined in A.3.1.2 for each specified crosstalk scenario defined in A.3.1.6.

NOTE – The injected noise is intended to match the theoretical noise PSD when the transceiver under test is connected to the loop. On Loop S for payload rates of 1024 kbit/s and below, and on all loops for payload rate of 192 kbit/s, it has been found that impedance mismatch could generate an increased noise PSD at low frequencies. One method of compensation is to modify the factor, Δ, defined in A.3.1.4 by replacing the theoretical noise, *N(f)*, in step 3 of A.3.1.4 with the noise PSD measured when connected to the loop under test. A second method is to place a passive circuit, consisting of a resistor R in parallel with a capacitor C, in series with each wire of the noise generator output pair. The RC values of R = 1.2 kΩ and C = 1 μF are suggested and should be adjusted for each noise generator such that the injected noise matches the theoretical noise PSD. A third method is to calibrate the noise generator waveform into the loop under test such that when connected to the loop under test, the theoretical noise waveform is present at the transceiver terminals.

A.3.1.4 Calibration of loop simulator

There is significant variation in loop insertion loss for the same loop model on loop simulators from both different and identical manufacturers. Typical loop simulators may exhibit insertion loss variations greater than ±1.0 dB of the ideal loop model over the SHDSL signal band. Insertion loss variation of loop simulators may cause significant variation of measured system noise margin. To minimize measurement variation caused by the loop simulator, the crosstalk generator output power may be adjusted to maintain a consistent SNR at the receiver input. The calibration procedure is as follows:

1) Given the discrete form of the DFE-based SNR formula, SNR_{dB}, given below:

$$SNR_{dB} = \frac{1}{M}\sum_{k=1}^{M} 10\log_{10}\left(1 + \frac{S(f_{sym}-f_k)\left|H(f_{sym}-f_k)\right|^2}{N(f_{sym}-f_k)} + \frac{S(f_k)\left|H(f_k)\right|^2}{N(f_k)} + \frac{S(2f_{sym}-f_k)\left|H(2f_{sym}-f_k)\right|^2}{N(2f_{sym}-f_k)} + \frac{S(f_{sym}-f_k)\left|H(f_{sym}-f_k)\right|^2}{N(f_{sym}-f_k)} \right)$$

calculate $SNR1$, the ideal receive signal-to-noise ratio, by setting $SNR1$ equal to SNR_{dB} where $S(f)$ shall be the nominal far-end transmit signal power spectral density (*NominalPSD(f)* from A.4), $|H(f)|^2$ shall be the magnitude squared of the ideal loop insertion gain function, $N(f)$ shall be the injected crosstalk noise power spectral density ($PSD_{Case\text{-}n}(f)$ from A.3.3.9), and f_{sym} shall be the transmit symbol rate. For this application use $f_k = k \times 1000$, $k = 1 \ldots M$, where M is the maximum value of k such that $M \times 1000 < f_{sym} \le (M + 1) \times 1000$. The ideal loop insertion gain function shall be calculated from the primary constants of twisted pair copper as defined in Annex A/G.996.1 [6].

2) Measure the insertion loss of the loop simulator with 135 Ω terminations at points f_k defined in step 1. Note that the termination return loss with respect to 135 Ω should be greater than 35 dB from 20 kHz to f_{sym} to ensure insertion loss measurement accuracy within 0.25 dB over the main part of the SHDSL signal band. An example insertion loss measurement set-up is shown in Figure A.3. The measured loss in dB of the loop at each frequency shall be within 5% (in dB) of the theoretical loop insertion loss function as calculated in step 1. As the measurements for the calibration procedure are easily made with error, the return loss measurement set used to verify the 35 dB return loss of the test fixture terminations shall be calibrated with a known return loss test load of at least 55 dB over the range of 20 kHz to 500 kHz. In addition, the line simulator should exhibit a longitudinal balance of 35 dB or better for frequencies in the range of 0 to f_{sym}.

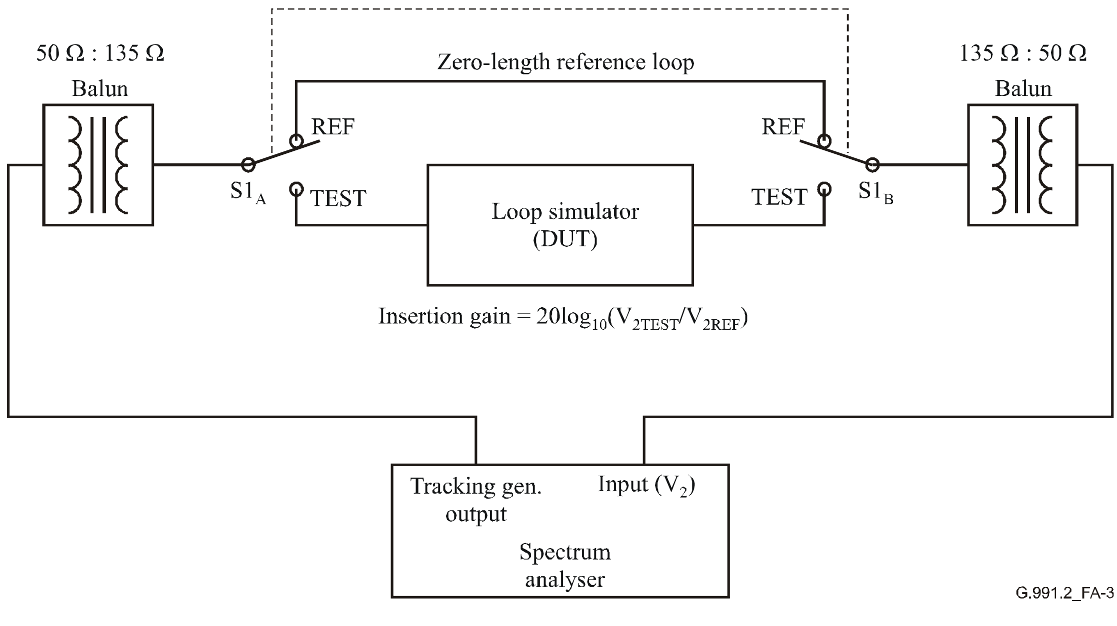


Figure A.3/G.991.2 – Example loop insertion loss measurement set-up

3) Calculate *SNR2*, the measured receive signal-to-noise ratio, by setting *SNR*2 equal to SNR_{dB} from step 1 where $|H(f)|^2$ is the magnitude squared of the measured loop insertion gain function from step 2 above, and $S(f)$, $N(f)$, f_{sym}, and f_k are the same as in step 1 above.

4) Adjust the noise margin target in Table A.1 by Δ = (SNR2 – SNR1) dB. Note that a negative difference corresponds to a decrease in crosstalk generator power. Note that this procedure assumes the crosstalk generator was previously calibrated as per A.3.1.2 and A.3.1.3. All crosstalk power adjustments shall be limited to 3.0 dB maximum. Test set-ups requiring greater than 3.0 dB crosstalk power adjustment shall not be valid.

A.3.1.5 Crosstalk margin compliance procedure

The SHDSL transceivers shall have noise margins that meet or exceed the values listed in Table A.1 for the specified test loop and crosstalk combinations. The definitions of the test loops are given in Figure A.1, and specifications for the crosstalk PSDs are given in A.3.3. The test for noise margin compliance shall be defined as follows:

1) Calibrate the crosstalk injection circuit (using the calibration load of 67.5 Ω) to the corresponding PSD and total power value specified in A.3.3.
2) Increase the injected crosstalk power by the corresponding noise margin value specified in Table A.1.
3) Using the test set-up from Figure A.2, activate the SHDSL transceivers and allow a minimum 5-minute fine-tuning period.
4) Measure the BER over a minimum of 10^9 bits.
5) The measured BER at each end shall be less than 10^{-7}.

A.3.1.6 Crosstalk interference requirements

Table A.1 shows the minimum set of test loops and crosstalk combinations required for testing SHDSL margins. A compliant unit shall pass the BER test described in A.3.1.5 for all crosstalk scenarios and test loops defined in Table A.1. 0 dB Power Backoff shall be used for both the STU-C and STU-R.

Table A.1/G.991.2 – Crosstalk scenarios & required SHDSL noise margins (Note)

Test	Test loop (from Figure A.1)	*L* (× 1000')	Test unit	Payload data rate (kbit/s)	PSD	Interferer combination	Required margin (dB)
1	C4	–	STU-C	1544	Asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
2	C4	–	STU-C	1544	Asymmetric	39 SHDSL	$5 + \Delta^*$
3	C4	–	STU-C	1544	Asymmetric	24 FDD ADSL + 24 HDSL	$5 + \Delta^*$
4	S	9.0	STU-C	1544	Asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
5	S	9.0	STU-C	1544	Asymmetric	39 SHDSL	$5 + \Delta^*$
6	S	9.0	STU-C	1544	Asymmetric	24 FDD ADSL + 24 HDSL	$5 + \Delta^*$
7	C4	–	STU-R	1544	Asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
8	S	9.0	STU-R	1544	Asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$

Table A.1/G.991.2 – Crosstalk scenarios & required SHDSL noise margins (Note)

Test	Test loop (from Figure A.1)	*L* (× 1000')	Test unit	Payload data rate (kbit/s)	PSD	Interferer combination	Required margin (dB)
9	S	6.3	STU-C	2304	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
10	BT1-C	5.2	STU-C	2304	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
11	BT1-C	5.2	STU-C	2304	Symmetric	49-SHDSL	5 + Δ*
12	S	6.3	STU-R	2304	Symmetric	49-SHDSL	5 + Δ*
13	BT1-R	5.2	STU-R	2304	Symmetric	49-SHDSL	5 + Δ*
14	BT1-R	5.2	STU-R	2304	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
15	S	6.8	STU-C	2048	Symmetric	24-SHDSL + 24-FDD ADSL	5 + Δ*
16	BT1-C	5.6	STU-C	2048	Symmetric	49-SHDSL	5 + Δ*
17	BT1-C	5.6	STU-C	2048	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
18	S	6.8	STU-R	2048	Symmetric	49-SHDSL	5 + Δ*
19	BT1-R	5.6	STU-R	2048	Symmetric	49-SHDSL	5 + Δ*
20	BT1-R	5.6	STU-R	2048	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
21	S	7.9	STU-C	1544	Symmetric	39-SHDSL asym 1544	5 + Δ*
22	BT1-C	6.4	STU-C	1544	Symmetric	24-FDD ADSL + 24 SHDSL asym 1544	5 + Δ*
23	BT1-C	6.4	STU-C	1544	Symmetric	24-SHDSL + 24-FDD ADSL	5 + Δ*
24	S	7.9	STU-R	1544	Symmetric	49-SHDSL	5 + Δ*
25	BT1-R	6.4	STU-R	1544	Symmetric	24-T1 + 24 SHDSL asym 1544	5 + Δ*
26	BT1-R	6.4	STU-R	1544	Symmetric	49-SHDSL	5 + Δ*
27	S	11.0	STU-C	768	Symmetric	49-HDSL	5 + Δ*
28	BT1-C	10.2	STU-C	768	Symmetric	49-SHDSL	5 + Δ*
29	BT1-C	10.2	STU-C	768	Symmetric	49-HDSL	5 + Δ*
30	S	11.0	STU-R	768	Symmetric	49-HDSL	5 + Δ*
31	BT1-R	10.2	STU-R	768	Symmetric	49-SHDSL	5 + Δ*
32	BT1-R	10.2	STU-R	768	Symmetric	49-HDSL	5 + Δ*

Table A.1/G.991.2 – Crosstalk scenarios & required SHDSL noise margins (Note)

Test	Test loop (from Figure A.1)	*L* (× 1000')	Test unit	Payload data rate (kbit/s)	PSD	Interferer combination	Required margin (dB)
33	S	11.2	STU-C	768	Asymmetric	49-HDSL	$5 + \Delta^*$
34	BT1-C	10.4	STU-C	768	Asymmetric	49-HDSL	$5 + \Delta^*$
35	BT1-C	10.4	STU-C	768	Asymmetric	24-FDD ADSL + 24-HDSL	$5 + \Delta^*$
36	S	11.2	STU-R	768	Asymmetric	24-T1 + 24 HDSL	$5 + \Delta^*$
37	BT1-R	10.4	STU-R	768	Asymmetric	24-T1 + 24-SHDSL	$5 + \Delta^*$
38	BT1-R	10.4	STU-R	768	Asymmetric	39-FDD ADSL	$5 + \Delta^*$
39	S	14.8	STU-C	384	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
40	BT2-C	13.8	STU-C	384	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
41	BT2-C	13.8	STU-C	384	Symmetric	49-SHDSL	$5 + \Delta^*$
42	S	14.8	STU-R	384	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
43	BT2-R	13.8	STU-R	384	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
44	BT2-R	13.8	STU-R	384	Symmetric	49-SHDSL	$5 + \Delta^*$
45	S	17.2	STU-C	256	Symmetric	49-DSL	$5 + \Delta^*$
46	BT2-C	16.4	STU-C	256	Symmetric	49-DSL	$5 + \Delta^*$
47	BT2-C	16.4	STU-C	256	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
48	S	17.2	STU-R	256	Symmetric	49-DSL	$5 + \Delta^*$
49	BT2-R	16.4	STU-R	256	Symmetric	49-DSL	$5 + \Delta^*$
50	BT2-R	16.4	STU-R	256	Symmetric	24-SHDSL + 24-DSL	$5 + \Delta^*$
51	S	19.8	STU-C	192	Symmetric	49-DSL	$5 + \Delta^*$
52	BT2-C	19.1	STU-C	192	Symmetric	49-DSL	$5 + \Delta^*$
53	BT2-C	19.1	STU-C	192	Symmetric	24-DSL + 24 SHDSL	$5 + \Delta^*$
54	S	19.8	STU-R	192	Symmetric	49-DSL	$5 + \Delta^*$
55	BT2-R	19.1	STU-R	192	Symmetric	49-DSL	$5 + \Delta^*$
56	BT2-R	19.1	STU-R	192	Symmetric	24-DSL + 24 SHDSL	$5 + \Delta^*$

NOTE – The crosstalk scenarios listed in this table were developed under the assumption of a 50-pair cable binder. Cable binders of other sizes are for further study.

* The indicated noise margins in Table A.1 shall have a tolerance of 1.25 dB due to the aggregate effect of crosstalk generator tolerance and calibrated loop simulator tolerance. The offset Δ is defined in A.3.1.4.

All interferers are assumed to be co-located. The notation 24 or 49 SHDSL refers to SHDSL at the same rate and PSD as the system under test. All interferer PSDs are described in A.3.3.9.

The process for selecting which tests to perform for a specific G.991.2 device under test (DUT) is determined by following each of these 6 steps in order:

1) Determine the set of rates which are in common between the set of supported payload data rates and the following set of payload data rates: (symmetric PSD: 192, 256, 384, 768, 1544, 2048, 2304 kbit/s; asymmetric PSD: 768, 1544 kbit/s). Call the resulting list of common rates the intersection list.
2) If 1544 kbit/s asymmetric is in the intersection list, then test the DUT with test cases 1-8 in Table A.1.
3) If 768 kbit/s asymmetric is in the intersection list, then test the DUT with test cases 33-38 in Table A.1.
4) If 1544 kbit/s symmetric is in the intersection list, then test the DUT with test cases 21-26.
5) For the highest and the lowest symmetric PSD rate in the intersection list, test the DUT with all six cases associated with that rate. For example, if 192 kbit/s symmetric is the lowest rate and 2304 kbit/s symmetric is the highest rate, then test with test cases 51-56 and 9-14 in Table A.1.
6) For all remaining rates in the intersection list that have not been tested, test using the cases involving only Loop S. For example, if 256, 384, 768 and 2048 kbit/s symmetric are the remaining rates, then test with the additional test cases 48, 45, 42, 39, 30, 27, 18 and 15.

If all rates are implemented by the DUT, there will be a total of 40 tests.

A.3.2 Impulse noise tests

A.3.2.1 Impulse noise test procedure

The impulse noise waveform V(t) (hereafter called the "test impulse") is defined as:

$$V(t) = \begin{Bmatrix} K|t|^{-3/4} & t > 0 \\ 0 & t = 0 \\ -K|t|^{-3/4} & t < 0 \end{Bmatrix}$$

where t is time given in units of seconds and K is a constant defined numerically in Table A.2. If the pulse is realized using discrete samples of $V(t)$, the waveform should be sampled at $t = (2n-1)\frac{T}{2}$, where T is the sampling period and ($1/T$) should be at least twice the symbol rate of the system under test. The sampled peak-to-peak amplitude will vary with sampling rate. It can be calculated using the following formula: $V_{p-p} = 2K\left|\frac{T}{2}\right|^{-\frac{3}{4}}$.

Table A.2/G.991.2 – Impulse noise peak-to-peak voltage requirement

K	V_{P-P} of the test impulse sampled at 2 Msamples/s
1.775×10^{-6}	320 mV

For a sampling rate of 2 Msamples/s, a minimum of 8000 samples is required with an amplitude accuracy of at least 12 bits. Figure A.4 shows the test impulse sampled at 2 Msamples/s. The injection circuit shall be identical to that described in A.3.1.

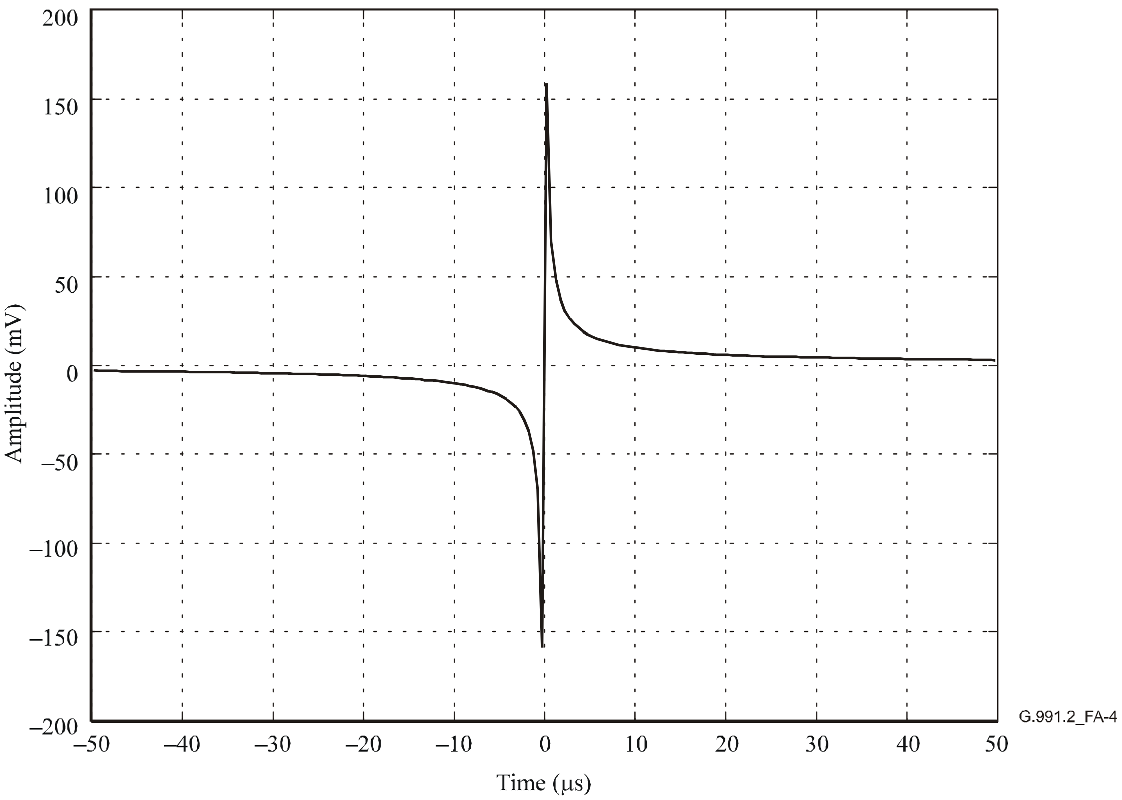


Figure A.4/G.991.2 – Time domain representation of the test pulse sampled at 2 Msamples/s

A.3.2.2 Impulse noise test performance

A compliant unit shall pass the impulse noise test specified in Table A.3. The minimum test period shall be 10 s. Each SHSDL termination shall be tested independently, i.e., the impulse noise waveform is not injected at both terminations simultaneously.

Table A.3/G.991.2 – Impulse noise test criteria

Test loop	Test pulse V_{P-P} when sampled at 2 Msamples/s	Test pulse repetition rate	Bit error ratio upper limit
Loop C4	320 mV	10 Hz	5.0×10^{-4}
Loop S, *L* = 9000'	320 mV	10 Hz	5.0×10^{-4}
NOTE – The entries in this table only correctly apply to the 1544 kbit/s asymmetric case. Appropriate values for other rates and PSDs are for further study.			

A.3.3 Power spectral density of crosstalk disturbers

A.3.3.1 Simulated HDSL PSD

The PSD of HDSL disturbers shall be expressed as:

$$PSD_{HDSL} = K_{HDSL} \times \frac{2}{f_0} \times \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\left(\frac{\pi f}{f_0}\right)} \right]^2 \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^8}, f_{3dB} = 196 \text{ kHz}, 0 \le f < \infty$$

where

$$f_0 = 392 \text{ kHz}, K_{HDSL} = \frac{5}{9} \times \frac{V_p^2}{R}, V_p = 2.70\text{V}, \text{and } R = 135\,\Omega$$

This equation gives the single-sided PSD; that is, the integral of PSD, with respect to *f*, from 0 to infinity, gives the power in Watts. PSD_{HDSL} is the PSD of a 392 ksymbol/s 2B1Q signal with random equiprobable levels, with full-band square-topped pulses and with 4th order Butterworth filtering ($f_{3\,dB}$ = 196 kHz).

A.3.3.2 Simulated T1 line PSD

The PSD of the T1 line disturber is assumed to be the 50% duty-cycle random Alternate Mark Inversion (AMI) code at 1.544 Mbit/s. The single-sided PSD shall be expressed as:

$$PSD_{T1} = \frac{V_p^2}{R_L} \times \frac{2}{f_0} \times \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\left(\frac{\pi f}{f_0}\right)} \right]^2 \sin^2\left(\frac{\pi f}{2 f_0}\right) \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^6} \times \frac{f^2}{f^2 + f_c^2}, 0 \le f < \infty$$

where

V_p = 3.6 V, R_L = 100 Ω, and f_0 = 1.544 MHz.

The formula assumes that transmitted pulses are passed through a low-pass shaping filter. The shaping filter is chosen as a 3rd order low-pass Butterworth filter with 3 dB point at 3.0 MHz. The filter magnitude squared transfer function is:

$$\left|H_{shaping}(f)\right|^2 = \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^6}$$

The formula also models the coupling transformer as a high-pass filter with 3 dB point at 40 kHz using:

$$\left|H_{Transformer}(f)\right|^2 = \frac{f^2}{f^2 + f_c^2}$$

A.3.3.3 Simulated ADSL downstream Frequency Division Duplex (FDD) PSD

The ADSL Downstream FDD PSD is based on the ATU-C transmitter PSD mask for reduced NEXT defined in Figure A.2/G.992.1 [1]. The simulated PSD used for SHDSL performance testing shall be defined as this G.992.1 mask reduced by 3.5 dBm/Hz over all frequencies.

A.3.3.4 Simulated ADSL upstream PSD

The ADSL Upstream PSD is based on the ATU-R transmitter PSD mask defined in Figure A.3/G.992.1 [1]. The simulated PSD used for SHDSL performance testing shall be defined as this G.992.1 mask reduced by 3.5 dBm/Hz over all frequencies.

A.3.3.5 Simulated SHDSL upstream PSD

The SHDSL Upstream PSD masks are defined in A.4. The simulated PSD used for SHDSL performance testing shall be the worst-case ensemble summation of the nominal upstream PSDs from A.4, with PBO set to 0 dB. The nominal PSD is given by the expression *NominalPSD(f)* in A.4.1, A.4.2 and A.4.3.

A.3.3.6 Simulated SHDSL downstream PSD

The SHDSL Downstream PSD masks are defined in A.4. The simulated PSD used for SHDSL performance testing shall be the worst-case ensemble summation of the nominal downstream PSDs from A.4, with PBO set to 0 dB. The nominal PSD is given by the expression *NominalPSD(f)* in A.4.1, A.4.2 and A.4.3.

A.3.3.7 Simulated DSL PSD

The power spectral density (PSD) of basic access DSL disturbers is expressed as:

$$PSD_{DSL\text{-}Disturber} = K_{DSL} \times \frac{2}{f_0} \times \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\left(\frac{\pi f}{f_0}\right)} \right]^2 \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^4},\ f_{3dB} = 80\ \text{kHz}, 0 \le f < \infty$$

where

$$f_0 = 80\ \text{kHz}, K_{DSL} = \frac{5}{9} \times \frac{V_p^2}{R}, V_p = 2.50\,\text{V}, \text{and}\ R = 135\,\Omega$$

This equation gives the single-sided PSD; that is, the integral of PSD, with respect to *f*, from 0 to infinity, gives the power in Watts. $PSD_{DSL\text{-}Disturber}$ is the PSD of an 80 ksymbol/s 2B1Q signal with random equiprobable levels, with full-band square-topped pulses and with 2nd order Butterworth filtering ($f_{3\,\text{dB}} = 80$ kHz).

A.3.3.8 NEXT

The NEXT power transfer function uses the two-piece Unger model which has a slope of 14 dB/decade for frequencies greater than 20 kHz and a slope of 4 dB/decade for frequencies less than or equal to 20 kHz. This is defined as follows where *N* is the total number of NEXT disturbers:

$$\left|H_{NEXT-2-Piece}(f,N)\right|^2 = \begin{cases} 4.6288 \times 10^{-10} \times f^{0.4} \times N^{0.6}, f \le 20\,kHz \\ 2.3144 \times 10^{-14} \times f^{1.4} \times N^{0.6}, f > 20\,kHz \end{cases}$$

The two-piece Unger model shall be used to model crosstalk when evaluating performance of the 1.536 or 1.544 Mbps asymmetric PSD.

The one-piece model for NEXT power transfer function is defined as follows where *N* is the total number of NEXT disturbers:

$$\left|H_{NEXT-1-Piece}(f,N)\right|^2 = 0.8536 \times 10^{-14} \times f^{1.5} \times N^{0.6}$$

The one-piece model shall be used to model crosstalk when evaluating performance for all rates and PSDs except the 1.536 or 1.544 Mbit/s asymmetric PSD.

The model for FEXT power transfer function is defined as follows where N is the total number of FEXT disturbers:

$$\left|H_{FEXT}(f,N,L,D)\right|^2 = \left|L(f)\right|^2 \times D \times 7.744 \times 10^{-21} \times f^2 \times N^{0.6}$$

where $L(f)$ is the insertion loss of the loop through which the interferer passes while the interferer and the signal under test are adjacent in the same binder, and D is the length of the loop in feet. The FEXT model shall be used to model crosstalk from asymmetric interferers (specifically 1.544 Mbit/s asymmetric and ADSL).

A.3.3.9 Crosstalk PSD definitions

The following PSD definitions are to be used to generate the crosstalk interferer combinations used for performance testing in Table A.1.

$$PSD_{Case-1} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 24, L_{C4}, 7600)\right|^2$$

$$PSD_{Case-2} = PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{NEXT-2-Piece}(f, 39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 39, L_{C4}, 7600)\right|^2$$

$$PSD_{Case-3} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{HDSL}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f, 24, L_{C4}, 7600)\right|^2$$

$$PSD_{Case-4} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{ADSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 24, L_{S9.0}, 9000)\right|^2$$

$$PSD_{Case-5} = PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{NEXT-2-Piece}(f, 39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 39, L_{S9.0}, 9000)\right|^2$$

$$PSD_{Case-6} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{HDSL}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f, 24, L_{S9.0}, 9000)\right|^2$$

$$PSD_{Case-7} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f, 24, L_{C4}, 7600)\right|^2$$

$$PSD_{Case-8} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-2-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f, 24, L_{S9.0}, 9000)\right|^2$$

$$PSD_{Case-9} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 24, L_{S6.3}, 6300)\right|^2$$

$$PSD_{Case-10} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 24, L_{BT1-C5.2}, 5200)\right|^2$$

$$PSD_{Case-11} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-12} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-13} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-14} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f, 24, L_{BT1-R5.2}, 5200)\right|^2$$

$$PSD_{Case-15} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-2048-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f, 24, L_{S6.8}, 6800)\right|^2$$

$$PSD_{Case-16} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-17} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 24, L_{BT1-C5.6}, 5600)\right|^2$$

$$PSD_{Case-18} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-19} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-20} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f, 24, L_{BT1-R5.6}, 5600)\right|^2$$

$$PSD_{Case-21} = PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{NEXT-1-Piece}(f, 39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f, 39, L_{S7.9}, 7900)\right|^2$$

$$PSD_{Case-22} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times |H_{NEXT-1-Piece}(f, 48)|^2 + \frac{24 \times PSD_{ADSL-Up}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times |H_{FEXT}(f, 48, L_{BT1-C6.4}, 6400)|^2$$

$$PSD_{Case-23} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-1544-Sym}(f)}{48} \times |H_{NEXT-1-Piece}(f, 48)|^2 + PSD_{ADSL-Up}(f) \times |H_{FEXT}(f, 24, L_{BT1-C6.4}, 6400)|^2$$

$$PSD_{Case-24} = PSD_{SHDSL-1544-Sym}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-25} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times |H_{NEXT-1-Piece}(f, 48)|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times |H_{FEXT}(f, 24, L_{BT1-R6.4}, 6400)|^2$$

$$PSD_{Case-26} = PSD_{SHDSL-1544-Sym}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-27} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-28} = PSD_{SHDSL-768-Sym}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-29} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-30} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-31} = PSD_{SHDSL-768-Sym}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-32} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-33} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-34} = PSD_{HDSL}(f) \times |H_{NEXT-1-Piece}(f, 49)|^2$$

$$PSD_{Case-35} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{HDSL}(f)}{48} \times |H_{NEXT-1-Piece}(f, 48)|^2 + PSD_{ADSL-Up}(f) \times |H_{FEXT}(f, 24, L_{BT_1-C10.4}, 10400)|^2$$

$$PSD_{Case-36} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{HDSL}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-37} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-768-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2 + PSD_{SHDSL-768-Asym-Down}(f) \times \left|H_{FEXT}(f, 24, L_{BT_1-R10.4}, 10400)\right|^2$$

$$PSD_{Case-38} = PSD_{ADSL-Up}(f) \times \left|H_{NEXT-1-Piece}(f, 39)\right|^2 + PSD_{ADSL-Down}(f) \times \left|H_{FEXT}(f, 39, L_{BT1-R10.4}, 10400)\right|^2$$

$$PSD_{Case-39} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-40} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-41} = PSD_{SHDSL-384-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-42} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-43} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-44} = PSD_{SHDSL-384-Sym}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-45} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-46} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-47} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-256-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-48} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-49} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-50} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-256-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-51} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-52} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-53} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-192-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

$$PSD_{Case-54} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-55} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f, 49)\right|^2$$

$$PSD_{Case-56} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-192-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f, 48)\right|^2$$

A.4 PSD masks

For all data rates, the measured transmit PSD of each STU shall not exceed the PSD masks specified in this clause ($PSDMASK_{SHDSL}(f)$), and the measured total power into 135 Ω shall fall within the range specified in this clause ($P_{SHDSL} \pm 0.5$ dB).

The inband PSD for $0 < f < 1.5$ MHz shall be measured with a 10 kHz resolution bandwidth.

NOTE – Large PSD variations over narrow frequency intervals (for example near the junction of the main lobe with the noise floor) might require a smaller resolution bandwidth (RBW) to be used. A good rule of thumb is to choose RBW such that there is no more than 1 dB change in the signal PSD across the RBW.

Support for the symmetric PSDs specified in A.4.1 shall be mandatory for all supported data rates. Support for the asymmetric PSDs specified in A.4.2 and A.4.3 shall be optional.

A.4.1 Symmetric PSD masks

For all values of framed data rate available in the STU, the following set of PSD masks ($PSDMASK_{SHDSL}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_{sym}} \times \frac{\left[\sin\left(\frac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\frac{\pi f}{N f_{sym}}\right)^2} \times \frac{1}{1 + \left(\frac{f}{f_{3dB}}\right)^{2 \times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.1\,\text{MHz} \end{cases}$$

where *MaskOffsetdB(f)* is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1 + 0.4 \times \frac{f_{3dB} - f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

f_{int} is the frequency where the two functions governing $PSDMASK_{SHDSL}(f)$ intersect in the range 0 to f_{sym}. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, *N*, f_{sym}, f_{3dB}, and P_{SHDSL} are defined in Table A.4. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload data rate.

Table A.4/G.991.2 – Symmetric PSD parameters

Payload data rate, R (kbit/s)	K_{SHDSL}	*Order*	N	f_{sym} (ksymbol/s)	f_{3dB}	P_{SHDSL} (dBm)
$R < 1536$	7.86	6	1	$(R + 8)/3$	$1.0 \times f_{sym}/2$	$P1(R) \le P_{SHDSL} \le 13.5$
1536 or 1544	8.32	6	1	$(R + 8)/3$	$0.9 \times f_{sym}/2$	13.5
$R > 1544$	7.86	6	1	$(R + 8)/3$	$1.0 \times f_{sym}/2$	13.5

$P1(R)$ is defined as follows:

$$P1(R) = 0.3486 \log_2 (R \times 1000 + 8000) + 6.06 \text{ dBm}$$

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure A.5 shows the PSD masks with 0 dB power backoff for payload data rates of 256, 512, 768, 1536, 2048 and 2304 kbit/s.

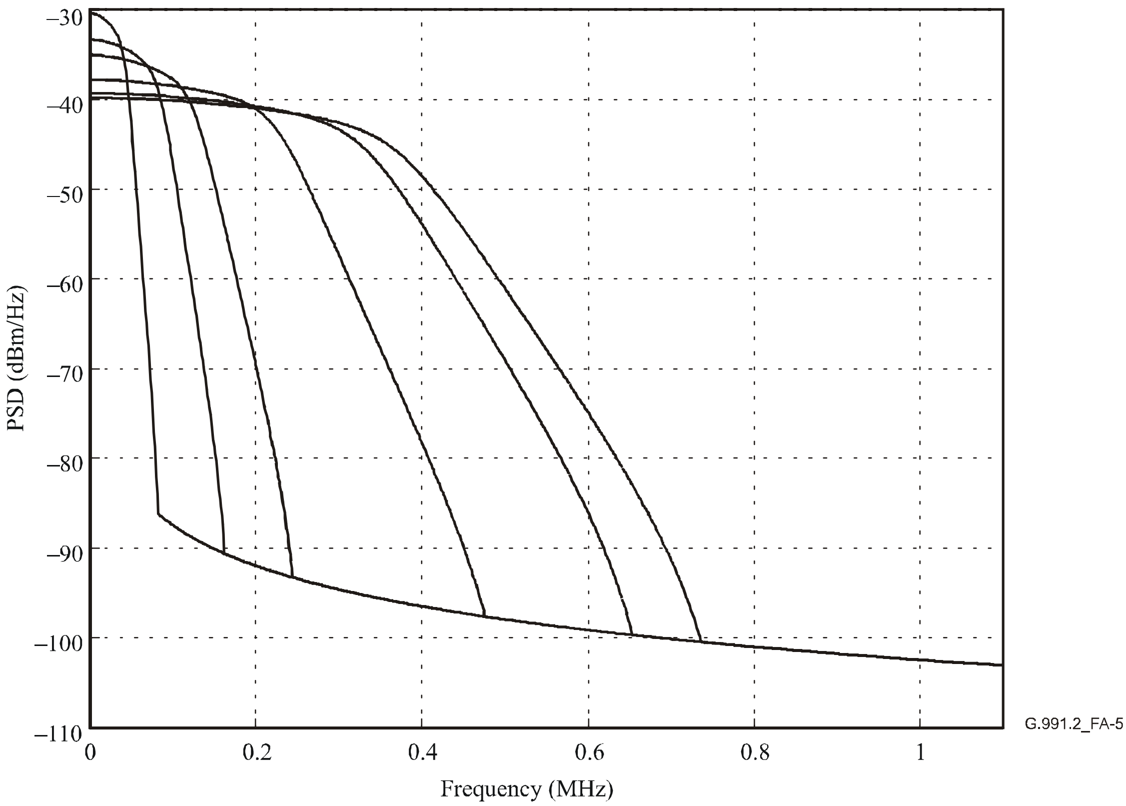


Figure A.5/G.991.2 – PSD masks for 0 dB power backoff

The equation for the nominal PSD measured at the terminals is:

$$NominalPSD(f) = \left\{ \begin{array}{l} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_{sym}} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\dfrac{\pi f}{N f_{sym}}\right)^2} \times \dfrac{1}{1 + \left(\dfrac{f}{f_{3dB}}\right)^{2 \times Order}} \times \dfrac{f^2}{f^2 + f_c^2}, f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5}, \quad f_{\text{int}} \le f \le 1.1 \text{MHz} \end{array} \right\}$$

where f_c is the transformer cut-off frequency, assumed to be 5 kHz. Figure A.6 shows the nominal transmit PSDs with 13.5 dBm power for payload data rates of 256, 512, 768, 1536, 2048 and 2304 kbit/s.

NOTE 1 – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see A.3.3.5 and A.3.3.6) as representative of typical implementations.

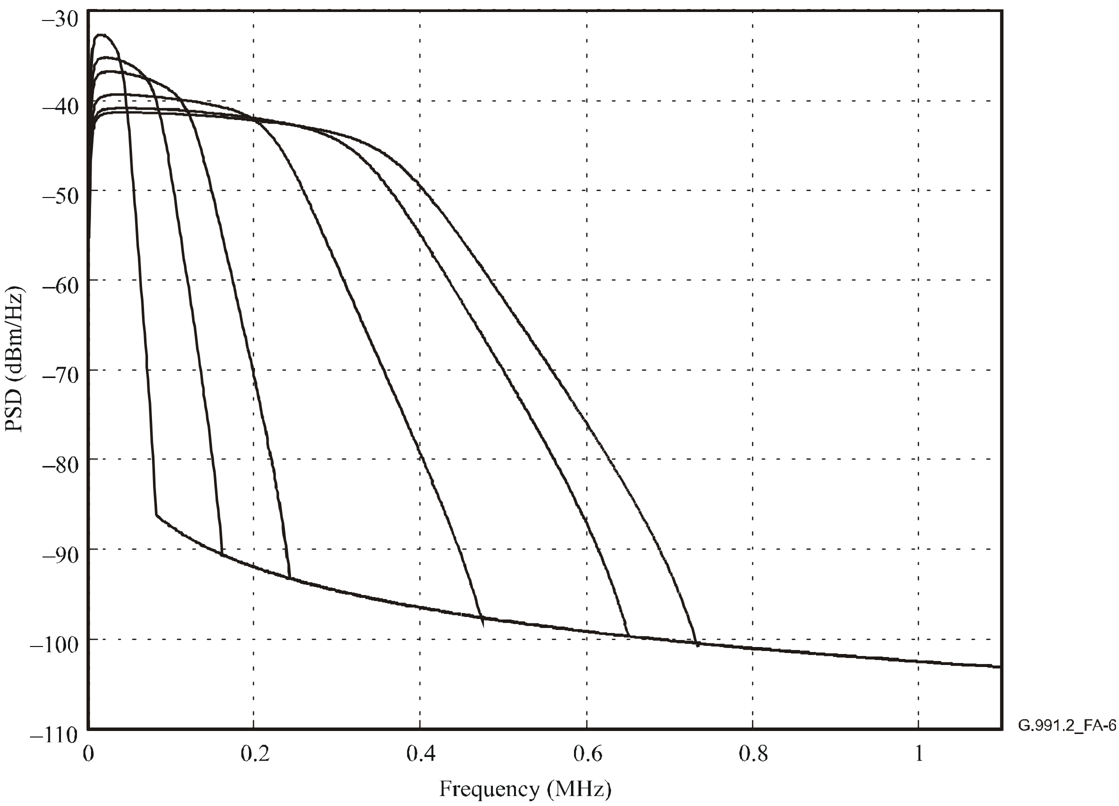


Figure A.6/G.991.2 – Nominal PSDs for 0 dB power backoff

NOTE 2 – In this clause, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz, and *f* is in units of Hz.

A.4.2 Asymmetric 1.536 or 1.544 PSD mask

The asymmetric PSD mask set specified in A.4.2.1 and A.4.2.2 shall optionally be supported for 1.536 and 1.544 Mbit/s payload data rates (1.544 and 1.552 Mbit/s framed data rates) in North America. The PSD masks are described for the 0 dB power backoff case. For other values of power backoff, the passband PSD masks shall shift, but the out-of-band mask shall remain constant. Power and power spectral density is measured into a load impedance of 135 Ω.

A.4.2.1 PSD mask for STU-C

For 0 dB power backoff, the output power of the STU-C during data mode shall be (16.8 ± 0.5) dBm in the frequency band from 0 to 440 kHz and shall be limited by the mask of Figure A.7. Table A.5 provides the numerical values for the mask of Figure A.7. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A.5.

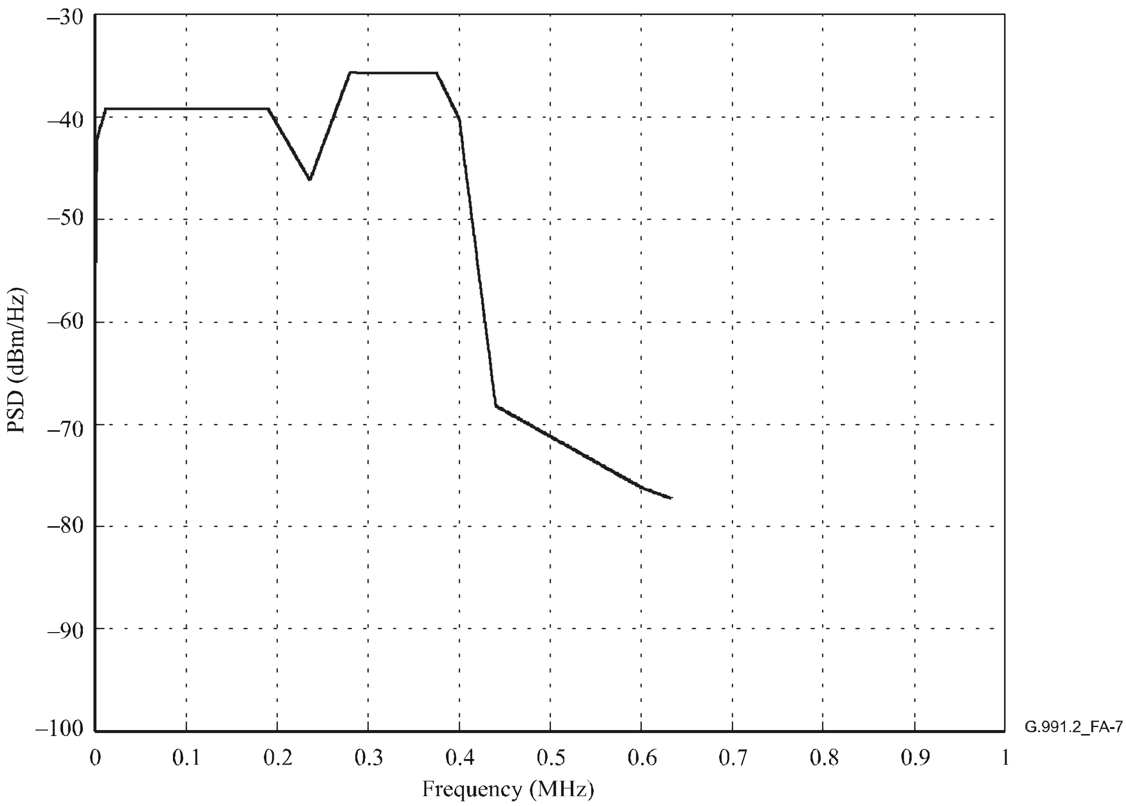


Figure A.7/G.991.2 – STU-C PSD mask for 1.536 or 1.544 Mbit/s with 0 dB power backoff

Table A.5/G.991.2 – STU-C PSD mask values for 1.536 or 1.544 Mbit/s with 0 dB power backoff

Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)
≤1	–54.2 – PBO	280	–35.7 – PBO	1000	–89.2
2	–42.2 – PBO	375	–35.7 – PBO	2000	–99.7
12	–39.2 – PBO	400	–40.2 – PBO	≥3000	–108
190	–39.2 – PBO	440	–68.2		
236	–46.2 – PBO	600	–76.2		

The STU-C PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A.5 for frequencies less than or equal to 400 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-C during data mode shall be (16.8 – *PBO* ± 0.5) dBm in the frequency band from 0 to 440 kHz. The power level during start-up shall be (16.6 – *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB.

NOTE – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see A.3.3.5 and A.3.3.6) as representative of typical implementations.

A.4.2.2 PSD mask for STU-R

For 0 dB power backoff, the output power of the STU-R during data mode shall be (16.5 ± 0.5) dBm in the frequency band from 0 to 300 kHz and shall be limited by the mask of Figure A.8. Table A.6 provides the numerical values for the mask of Figure A.8. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A.6.

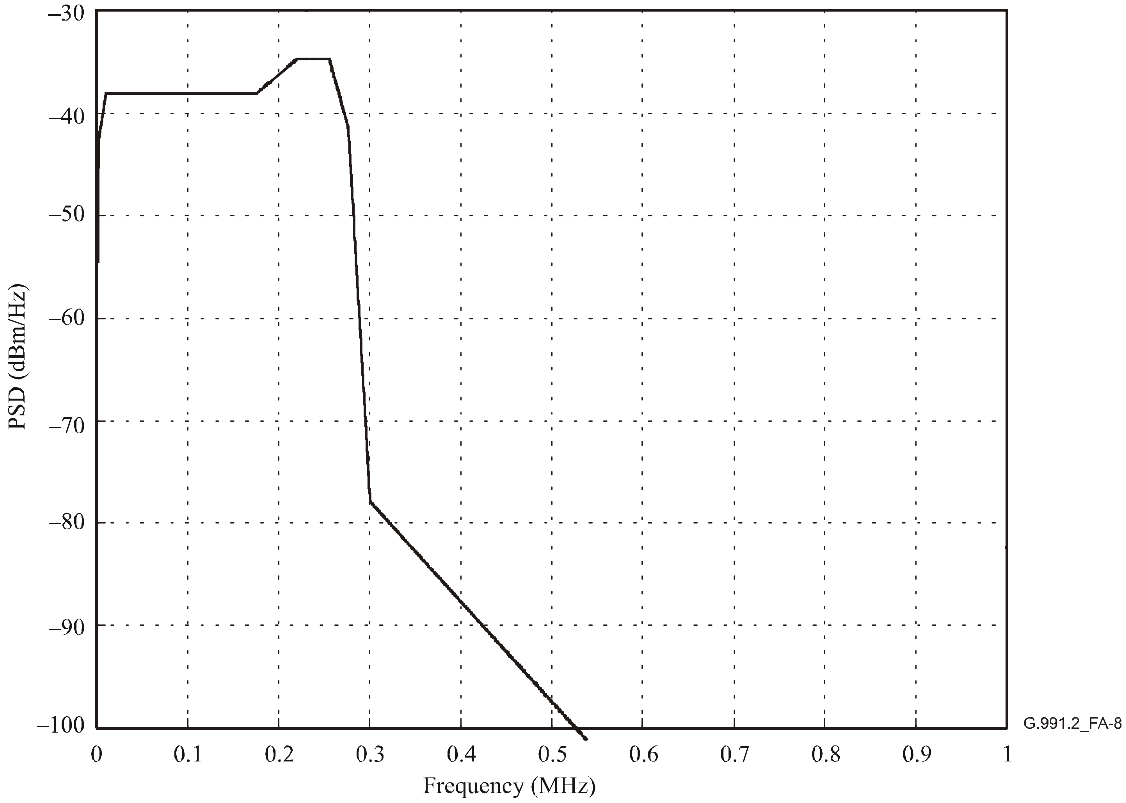


Figure A.8/G.991.2 – STU-R PSD Mask for 1.536 or 1.544 Mbit/s with 0 dB power backoff

Table A.6/G.991.2 – STU-R PSD mask values for 1.536 or 1.544 Mbit/s with 0 dB power backoff

Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)
≤1	–54.2 – PBO	220	–34.4 – PBO	555	–102.6
2	–42.1 – PBO	255	–34.4 – PBO	800	–105.6
10	–37.8 – PBO	276	–41.1 – PBO	1400	–108
175	–37.8 – PBO	300	–77.6	≥2000	–108

The STU-R PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A.6 for frequencies less than or equal to 276 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-R during data mode shall be (16.5 – *PBO* ± 0.5) dBm in the frequency band from 0 to 300 kHz. The power level during start-up shall be (16.3 – *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB.

NOTE – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see A.3.3.5 and A.3.3.6) as representative of typical implementations.

A.4.3 Asymmetric PSD masks for 768 or 776 kbit/s data rates

The asymmetric PSD mask set specified in A.4.3.1 and A.4.3.2 shall optionally be supported for the 768 kbit/s and 776 kbit/s payload data rates (776 and 784 kbit/s framed data rates) in North America. The PSD masks are described for the 0 dB power backoff case. For other values of power backoff, the passband PSD masks shall shift, but the out-of-band mask shall remain constant. Power and power spectral density is measured into a load impedance of 135 Ω.

A.4.3.1 PSD mask for STU-C

For 0 dB power backoff, the output power of the STU-C during data mode shall be (14.1 ± 0.5) dBm in the frequency band from 0 to 600 kHz and shall be limited by the mask of Figure A.9. Table A.7 provides the numerical values for the mask of Figure A.9. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A.7.

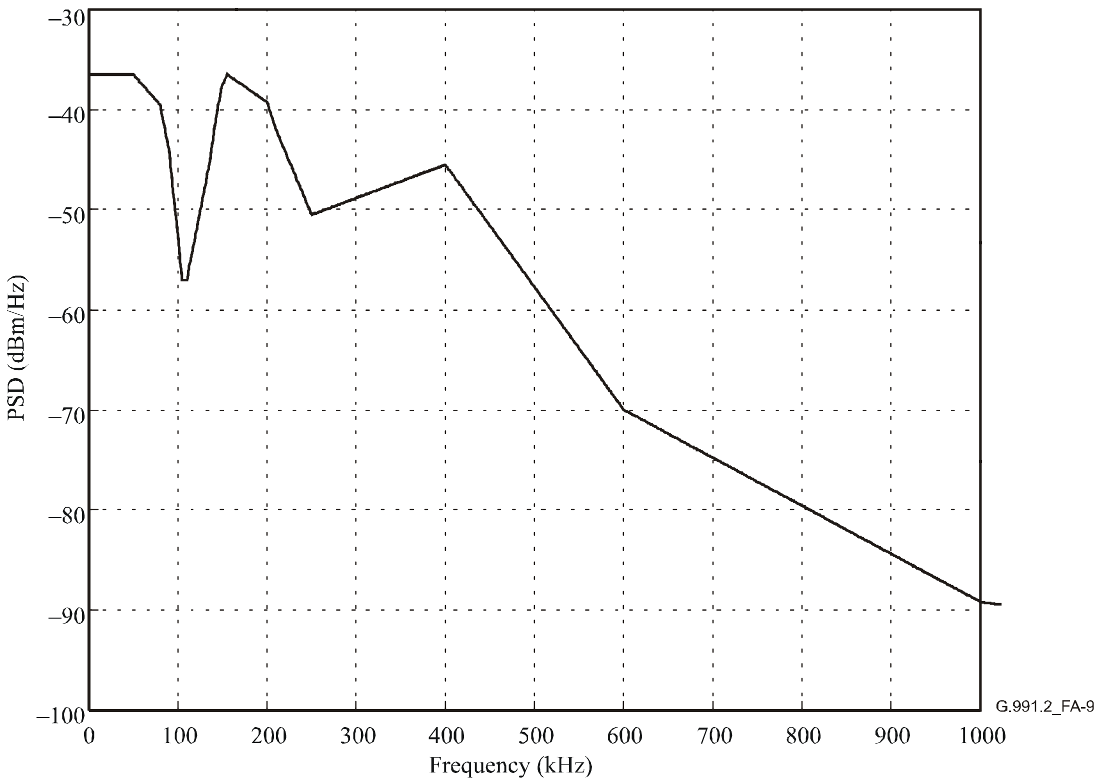


Figure A.9/G.991.2 – STU-C PSD mask for 768 or 776 kbit/s with 0 dB power backoff

Table A.7/G.991.2 – STU-C PSD mask values for 768 or 776 kbit/s with 0 dB power backoff

Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)	Frequency (kHz)	Maximum power (dBm/Hz)
≤50	–36.5 – PBO	135	–45.5 – PBO	250	–50.5 – PBO
80	–39.5 – PBO	145	–39.5 – PBO	400	–45.5 – PBO
90	–44 – PBO	150	–37.5 – PBO	600	–70
105	–57 – PBO	155	–36.5 – PBO	1000	–89.2
110	–57 – PBO	200	–39.25 – PBO	2000	–99.7
		210	–42 – PBO	≥3000	–108

The STU-C PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A.7 for frequencies less than or equal to 400 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-C during data mode shall be (14.1 – *PBO* ± 0.5) dBm in the frequency band from 0 to 600 kHz. The power level during start-up shall be (13.9 – *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB, multiplied by $f^2/(f^2 + f_c^2)$ where f is the frequency in Hz and f_c is 5000 Hz, the nominal transformer cut-off frequency.

NOTE – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see A.3.3.5 and A.3.3.6) as representative of typical implementations.

A.4.3.2 PSD mask for STU-R

For 0 dB power backoff, the output power of the STU-R during data mode shall be (14.1 ± 0.5) dBm in the frequency band from 0 to 300 kHz and shall be limited by the mask of Figure A.10. Table A.8 provides the equations for the mask of Figure A.10.

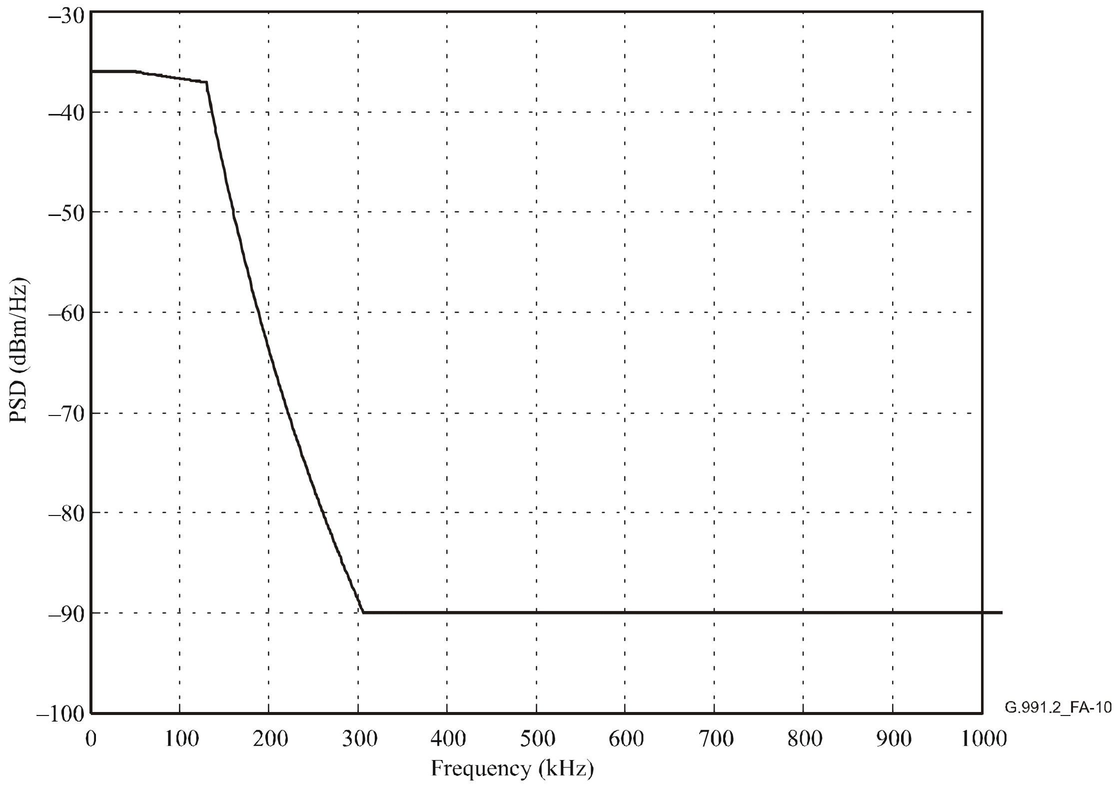


Figure A.10/G.991.2 – STU-R PSD mask for 768 or 776 kbit/s with 0 dB power backoff

Table A.8/G.991.2 – STU-R PSD mask values for 768 or 776 kbit/s with 0 dB power backoff

Frequency, f (Hz)	Maximum power (dBm/Hz)
$0 < f \le 50\,000$	–36 – PBO
$50\,000 < f \le 125\,000$	–36 – PBO – ((f – 50 000)/75 000)
$125\,000 < f \le 130\,000$	–37 – PBO
$130\,000 < f \le 307\,000$	$-37 - PBO - 142 \log_{10}(f/130\,000)$
$307\,000 < f \le 1\,221\,000$	–90
$1\,221\,000 < f \le 1\,630\,000$	–90 peak, with max power in the [f, f + 1 MHz] window of $(-90 - 48 \log_2(f/1\,221\,000) + 60)$ dBm
$f > 1\,630\,000$	–90 peak, with max power in the [f, f + 1 MHz] window of –50 dBm

The STU-R PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A.8 for frequencies less than or equal to 307 kHz, then by evaluation of the equations for power (dBm/Hz) over all frequencies. The output power of the STU-R during data mode shall be (14.1 – *PBO* ± 0.5) dBm in the frequency band from 0 to 307 kHz. The power level during start-up shall be (13.9 – *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB, multiplied by $f^2/(f^2 + f_c^2)$ where f is the frequency in Hz and f_c is 5000 Hz, the nominal transformer cut-off frequency.

NOTE – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see A.3.3.5 and A.3.3.6) as representative of typical implementations.

A.5 Region-specific functional characteristics

A.5.1 Data rate

The operation of the STU in data mode at the specified information rate shall be as specified in Table A.9.

Table A.9/G.991.2 – Framed data mode rates

Payload data rate, *R* (kbit/s)	Modulation	Symbol rate (ksymbol/s)	*K* (Bits per symbol)
$R = n \times 64 + (i) \times 8$	16-TCPAM	$(R + 8) \div 3$	3

For devices supporting Annex A functionality, no additional limitation on data rates shall be placed beyond the limitations stated in clause 5 and reiterated in 7.1.1, 8.1 and 8.2.

A.5.2 Return loss

For devices supporting Annex A functionality, return loss shall be specified based on the methodology of 11.3 and the limitations of Figure 11-6. The following definitions shall be applied to the quantities shown in Figure 11-6:

$$RL_{MIN} = 12 \text{ dB}$$

$$f_0 = 12.56 \text{ kHz}$$

$$f_1 = 50 \text{ kHz}$$

$$f_2 = f_{sym}/2$$

$$f_3 = 1.99\, f_{sym}$$

where f_{sym} is the symbol rate.

A.5.3 Span powering

The capability for an STU-C to provide power over a span to an STU-R is optional. However, if this capability is provided, the STU-C shall meet the requirements of A.5.3.1. The capability for an STU-R (or an SRU) to be remotely powered over the span is optional. However, if this capability is provided, the STU-R or SRU shall meet the requirements of A.5.3.2. Segments that do not support span powering or that have it disabled may optionally provide wetting (sealing) current, as defined in A.5.3.3.

The STU-C, STU-R and SRU shall comply with all applicable industry safety standards that are consistent with their deployment. In particular, it is highly desirable that SHDSL equipment comply with ITU-T Rec. K.50 [B4].

If an STU-R is deployed as CPE (i.e., it is part of a subscriber's installation), then span powering shall be disabled at the STU-C. The STU-C may optionally provide wetting current, as specified in A.5.3.3.

When implemented, SHDSL span powering shall support DC powering of remote terminal units over single-span loop resistances from 0 to 1800 Ω. The maximum span resistance shall include the worst-case loop resistance plus the wiring inside the central office and remote site. The STU-C span power supply shall be designed as a voltage source and shall be considered a voltage-limited circuit in the application of all referenced standards.

The span powering requirements defined herein are intended for use across a single segment from an STU-C to either an STU-R or an SRU. Application of these requirements in the STU-C to SRU case shall result in the termination of span powering voltages at the SRU. Succeeding segments may optionally support wetting current. Powering across multiple spans is not prohibited; however, the requirements are for further study. Wetting current may optionally be supported across any segment (STU-R to STU-C, STU-C to SRU, SRU to STU-R or SRU to SRU-R).

To ensure interoperability and reliable operation, the STU-C and STU-R (or SRU) shall meet the following requirements when span powering is implemented:

A.5.3.1 STU-C span powering source

A.5.3.1.1 Output voltage

The maximum potential between tip and ring shall be 200 V. The minimum potential between tip and ring shall be 160 V.

A.5.3.1.2 Power

The minimum steady-state power output capability shall be 15 W.

A.5.3.1.3 Polarity

The negative potential shall be applied to the terminal designated "ring" or "R". The potential from tip-to-ground should be zero or negative.

A.5.3.1.4 Slew Rate

The supply voltage power-up slew rate at the STU-C loop interface (rise time of V_{TEST}) shall be at least 1 V/ms but no greater than 30 V/ms when measured in the test circuit of Figure A.11 under all test conditions defined in Table A.10.

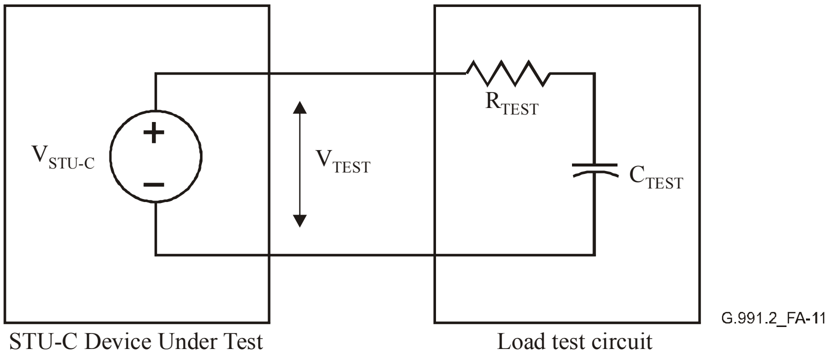


Figure A.11/G.991.2 – STU-C power-up slew rate test circuit

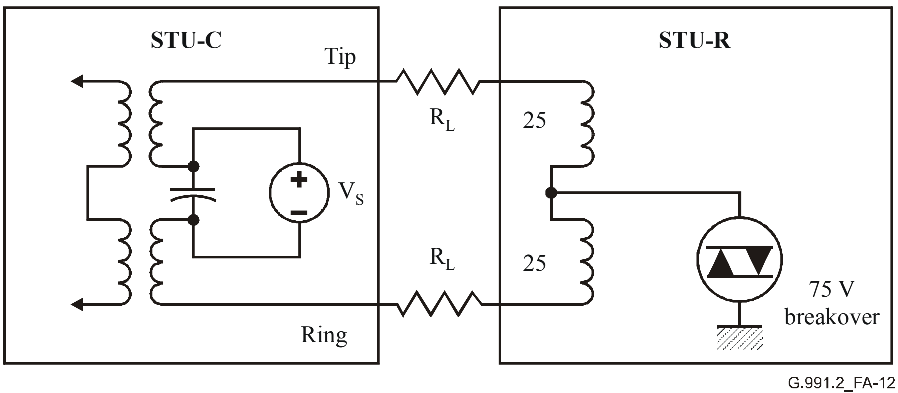
Table A.10/G.991.2 – Test conditions for STU-C slew rate

C_{TEST} (µF)	R_{TEST} (Ω)
1.0	100
1.0	1800
15	100
15	1800

NOTE (informative) – On a 900 Ω loop, the STU-C output voltage specification results in a maximum remote power load of 7.1 W.

A.5.3.1.5 Power feeding oscillation

The STU-C power supply should be designed to ensure that power feeding oscillation (a condition that could result in excessive noise coupling into other wire pairs in the cable) does not occur for the electrical characteristics shown for the protection circuit in Figure A.12.



NOTE (informative) – With appropriate current (to ground) restrictions, these requirements are not in conflict with the criteria of the Class 2 Voltage limits contained in [B5].

Figure A.12/G.991.2 – Power oscillation example circuit

A.5.3.2 STU-R (and SRU) powering

A.5.3.2.1 Input voltage

The STU-R (or SRU) shall operate properly over the range of input voltages from 80 V to 200 V. The STU-R (or SRU) may operate with input voltages less than 80 V.

A.5.3.2.2 Polarity

An STU-R (or SRU) shall function normally independent of the polarity of the line power input voltage. Note that tip/ring reversal is indicated via the EOC by the Maintenance Status Response message (9.5.5.7.20).

A.5.3.2.3 Capacitance

The capacitance of the STU-R (or SRU) shall be less than or equal to 15 µF.

A.5.3.2.4 Load characteristic

In order to guarantee power system stability during power-up and steady-operation, STU-R (or SRU) shall present a load characteristic which produces the following observable measurements when inserted in the test circuit shown in Figure A.13.

While V_{LINE} is ramped up from 0 V to the specified maximum voltage at the specified slew rate, the values of V_{LINE} and V_{LOAD} shall be observed and recorded. Set t_0 as the recorded time point during the power-up sequence when $V_{LOAD} = V_{LINE}/2$. The load characteristic of the STU-R (or SRU) device under test (DUT) shall be such that for all time $t > t_0$, $V_{LOAD} > V_{LINE}/2$. This criteria shall be met for all test conditions defined in Table A.11.

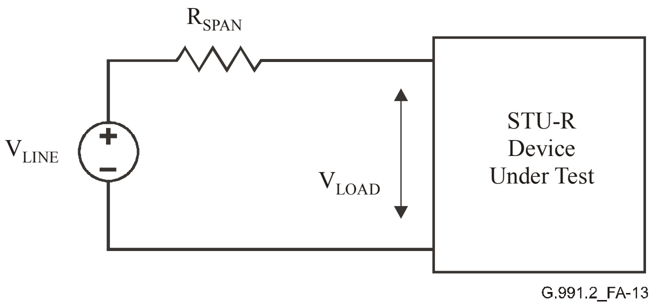


Figure A.13/G.991.2 – Test circuit for STU-R turn-on load characteristic

Table A.11/G.991.2 – Test conditions for STU-R turn-on load characteristic

V_{LINE} slew rate (V/ms)	V_{LINE} maximum voltage	R_{SPAN} (Ω)
1.0	200	100
1.0	160	1800
30.0	200	100
30.0	160	1800

The test power supply used to generate V_{LINE} should have a minimum load capacity of 20 W at all output voltages up to 200 V. The test power supply should use linear voltage regulation to minimize transient output voltage effects (observed at V_{LINE}) in the presence of test load variations.

A.5.3.3 Wetting current

The STU-R (or SRU-R) shall be capable of drawing between 1.0 and 20 mA of wetting (sealing) current from the remote feeding circuit when span powering is disabled or is not supported. The maximum rate of change of the wetting current shall be no more than 20 mA per second.

The STU-C (or SRU-C) may optionally supply power to support wetting current if span powering is disabled or is not supported. When enabled, this power source should produce a nominal –48 V potential measured at ring with respect to tip. The maximum voltage of the power source (if provided) should be limited to –56.5 V. The minimum voltage should be high enough to ensure a voltage of at least –39 V at the inputs of the STU-R (or SRU-R), measured at ring with respect to tip, to guarantee that the STU-R (or SRU-R) metallic termination will turn on and allow wetting current to flow. In no case shall the wetting current source apply a potential greater than –72 V between ring and tip. The potential at tip with respect to ground should be zero or negative.

A.5.3.4 Metallic termination

A metallic termination at the STU-R shall be provided in conjunction with the use of wetting current (A.5.3.3). The SRU-R shall meet the same requirements specified in this clause for an STU-R.

Table A.12 and Figure A.14 give characteristics that apply to the DC metallic termination of the STU-R. The metallic termination provides a direct current path from tip to ring at the STU-R, providing a path for sealing current. By exercising the non-linear functions of the metallic termination, a network-side test system may identify the presence of a conforming STU-R on the customer side of the interface. The characteristics of the metallic termination shall not be affected by whether the STU-R is powered in any state, or unpowered.

There are two operational states of the DC metallic termination:

a) the ON or conductive state; and

b) the OFF or non-conductive state.

A.5.3.4.1 ON state

The application of a voltage across the metallic termination greater than V_{AN}, the activate/non-activate voltage, for a duration greater than the activate time shall cause the termination to transition to the ON state. The activate/non-activate voltage shall be in the range of 30.0 to 39.0 V. The activate time shall be in the range of 3.0 to 50.0 ms. If a change of state is to occur, the transition shall be completed within 50 ms from the point where the applied voltage across the termination first exceeds V_{AN}. Application of a voltage greater than V_{AN} for a duration less than 3.0 ms shall not cause the termination to transition to the ON state. See Table A.12 and Figure A.14.

While in the ON state, when the voltage across the termination is 15 V, the current shall be greater than or equal to 20 mA. The metallic termination shall remain in the ON state as long as the current is greater than the threshold I_{HR} (see Table A.12 and Figure A.14) whose value shall be in the range of 0.1 to 1.0 mA. Application of 90.0 V through 200 to 4000 Ω (for a maximum duration of 2 s) shall result in a current greater than 9.0 mA.

A.5.3.4.2 OFF state

The metallic termination shall transition to the OFF state if the current falls below the threshold I_{HR} whose value shall be in the range of 0.1 to 1.0 mA for a duration greater than the "guaranteed release" time (100 ms) (see Table A.12 and Figure A.14). If a change of state is to occur, the transition shall be completed within 100 ms from the point where the current first falls below I_{HR}. If the current falls below I_{HR} for a duration less than 3.0 ms, the termination shall not transition to the OFF state. While in the OFF state, the current shall be less than 5.0 µA whenever the voltage is less than 20.0 V. The current shall not exceed 1.0 mA while the voltage across the termination remains less than the activate voltage.

Descriptive material can be found in Table A.12 and Figure A.14.

A.5.3.4.3 STU-R capacitance

While the metallic termination is OFF, the tip-to-ring capacitance of the STU-R when measured at a frequency of less than 100 Hz shall be 1.0 µF ± 10%.

A.5.3.4.4 Behaviour of the STU-R during metallic testing

During metallic testing, the STU-R shall behave as follows:

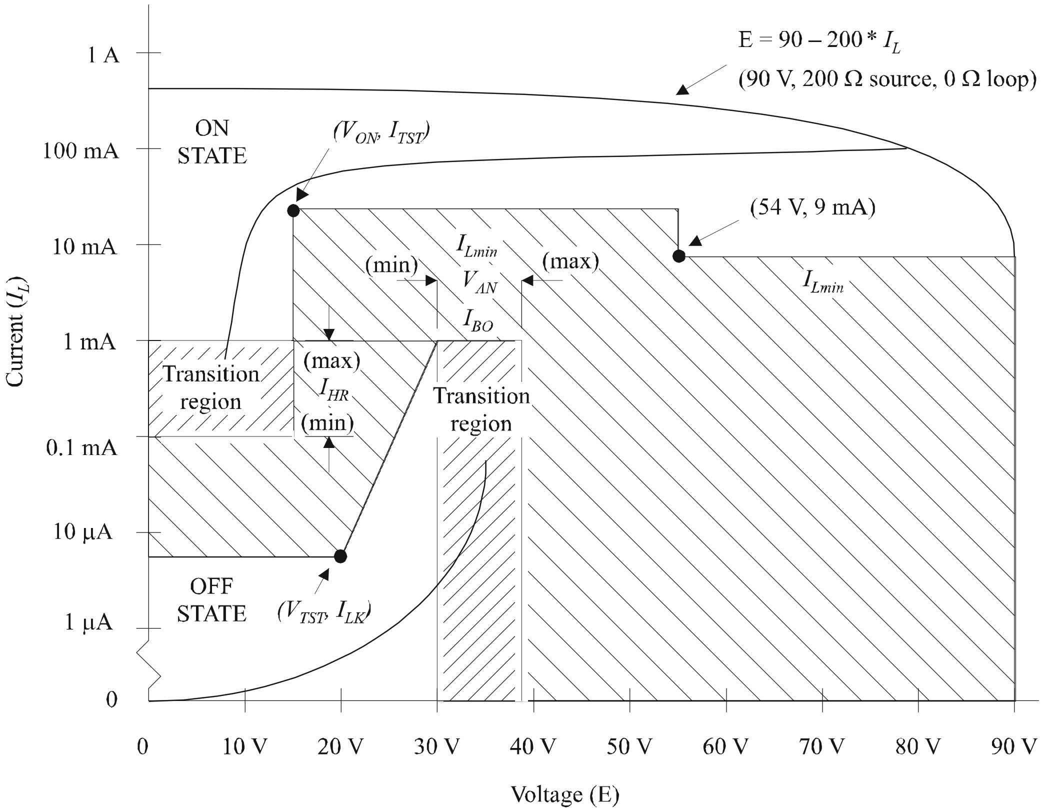
a) when a test voltage of up to 90 V[2] is applied across the loop under test, the STU-R shall present its DC metallic termination as defined in A.5.3.4, Table A.12 and Figure A.14, and not trigger any protective device that will mask this signature. The series resistance (test system + test trunk + loop + margin) can be from 200 to 4000 Ω (balanced between the two conductors);

b) the STU-R may optionally limit current in excess of 25 mA (20 mA maximum sealing current + 5 mA implementation margin).

Table A.12/G.991.2 – Characteristics of DC metallic termination at the STU-R

Type of operation	Normally OFF DC termination. Turned ON by application of metallic voltage. Held ON by loop current flow. Turned OFF by cessation of loop current flow.
Current in the ON state and at 15 V	≥ 20 mA
DC voltage drop (when ON) at 20 mA current	≤ 15 V
DC current with application of 90 V through 4000 Ω for up to 2 s.	min 9 mA (Note). See Figure A.14.
DC leakage current (when OFF) at 20 V	≤ 5.0 µA
Activate/non-activate voltage	30.0 V DC ≤ V_{AN} ≤ 39.0 V DC
Activate (breakover) current at V_{AN}	≤ 1.0 mA
Activate time for voltage ≥ V_{AN}	3 ms to 50 ms
Hold/release current	0.1 mA ≤ I_{HR} ≤ 1.0 mA
Release/non-release time for current ≤ I_{HR}	3 ms to 100 ms
NOTE – This requirement is intended to ensure a termination consistent with test system operation.	

[2] One test system in common use today applies 70 V DC plus 10 Vrms AC (84.4 V peak) to one conductor of the loop while grounding the other conductor.



DC Characteristics (EITHER POLARITY)

Parameter	Meaning	Limit	Condition	Meaning
I_{LK}	Leakage current	$I_{LT} \leq 5$ µA	$V_{TST} = 20\ V$	Test voltage
V_{AN}	Activate/Non-activate voltage	30 V ≤ V_{AN} ≤ 39 V		
I_{BO}	Break over current	$I_{BO} \leq 1.0$ mA		
I_{HR}	Hold/Release current	0.1 mA ≤ I_{HR} ≤ 1.0 mA		
V_{ON}	ON voltage	$V_{ON} \leq 15$ V	$I_{TST} = 20\ V\ mA$	Test current
I_{Lmin}	Minimum ON current	9 mA	54 V	

G.991.2_FA-14

Figure A.14/G.991.2 – Illustration of DC characteristics of the STU-R (Bilateral switch and holding current)

A.5.4 Longitudinal Balance

For devices supporting Annex A functionality, longitudinal balance shall be specified based on the methodology of 11.1 and the limitations of Figure 11-2. The following definitions shall be applied to the quantities in Figure 11-2.

$$LB_{MIN} = 40 \text{ dB}$$

$$f_1 = 20 \text{ kHz}$$

$$f_2 = f_{sym}/2$$

where f_{sym} is the symbol rate.

A.5.5 Longitudinal output voltage

For devices supporting Annex A functionality, longitudinal output voltage shall be specified based on the methodology of 11.2. The measurement frequency range shall be between 20 kHz and 450 kHz.

A.5.6 PMMS target margin

If the optional line probe is selected during the G.994.1 session, the receiver shall use the negotiated target margin. If worst-case PMMS target margin is selected, then the receiver shall assume the disturbers of Table A.13 to determine if a particular rate can be supported. Reference crosstalk shall be computed as defined in A.3.3 with the FEXT components in A.3.3.9 ignored. The reference crosstalk specified in this clause may not be representative of worst-case conditions in all networks. Differences between crosstalk environments may be compensated by adjusting the target margin.

Table A.13/G.991.2 – Reference disturbers used during PMMS for worst-case target margin

Rate (kbit/s)	PSD (direction)	Reference disturber
All	Symmetric (US/DS)	49 SHDSL
768/776	Asymmetric (US)	49 HDSL
768/776	Asymmetric (DS)	24 T1 + 24 HDSL
1536/1544	Asymmetric (US)	39 SHDSL (NEXT only)
1536/1544	Asymmetric (DS)	24 T1 + 24 SHDSL (NEXT only)

A.5.7 Span powering in *M*-pair mode

In the optional *M*-pair mode, the requirements for remote power feeding or wetting current for each of the *M* pairs shall be identical to the requirements for a single pair specified in A.5.3.

NOTE – This implies that the powering/wetting current is provided by a potential difference between tip and ring on each of the *M* pairs.

Annex B

Regional requirements – Region 2

B.1 Scope

This annex describes those specifications that are unique to SHDSL systems operating under conditions such as those typically encountered within European networks. The clauses in this annex provide the additions and modifications to the corresponding clauses in the main body.

B.2 Test loops

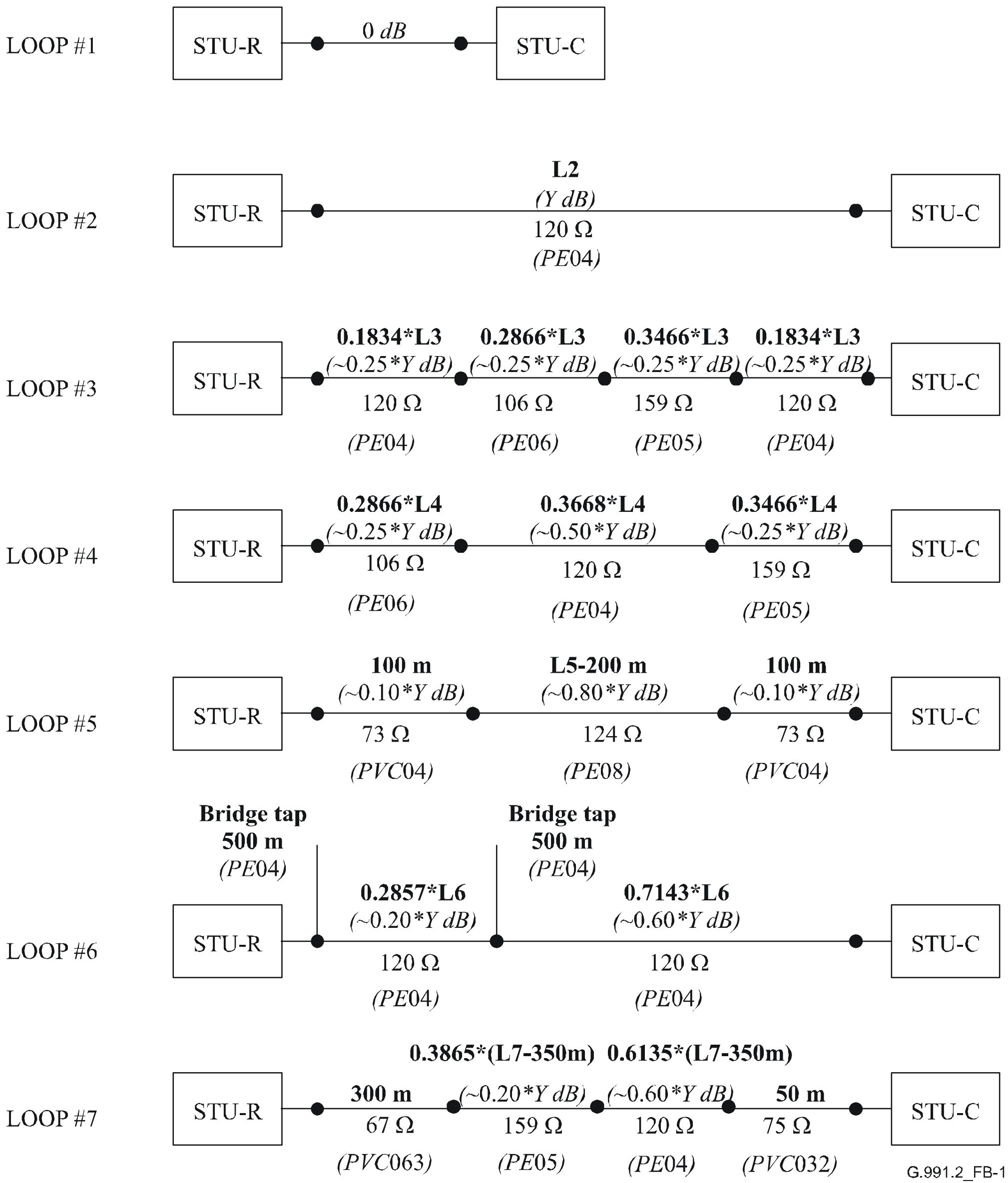
B.2.1 Functional description

The test loops in Figure B.1 are based on the existing HDSL test loops. The length of the individual loops are chosen such that the transmission characteristics of all loops are comparable. The purpose is to stress the equalizer of the SHDSL unit under test similarly over all loops when testing SHDSL at a specific bit rate. The total length of each loop is described in terms of *physical* length, and the length of the individual sections as a fixed fraction of this total. If implementation tolerances of one test loop causes its resulting *electrical* length to be out of specification, then its total physical length shall be scaled accordingly to correct this error. One test loop includes bridged taps to achieve rapid variations in amplitude and phase characteristics of the cable transfer function. In some access networks, these bridge taps have been implemented in the past, which stresses the SHDSL modem under test differently.

Loop #1 is a symbolic name for a loop with zero (or near zero) length, to prove that the SHDSL transceiver under test can handle the potentially high signal levels when two transceivers are directly interconnected.

B.2.2 Test loop topology

The topology of the test loops is specified in Figure B.1. The basic test cable characteristics, the transfer function of the test loops specified using these cables and the variation of input impedance of the test loops are shown in Appendix II.



NOTE 1 – The values for Y and L are to be found in Table B.1.
NOTE 2 – Due to mismatches and bridged taps, the total attenuation of the test loops differs from the sum of the attenuation of the parts.
NOTE 3 – The impedances are for information only. They refer to the characteristic impedances of the test cables as defined in Appendix II measured at 300 kHz.

Figure B.1/G.991.2 – Test loop topology

B.2.3 Test loop length

The length of each test loop for SHDSL transmission systems is specified in Table B.1. The specified insertion loss Y at the specified test frequency measured with a 135 Ω termination (*electrical* length) is mandatory. If implementation tolerances of one test loop causes that its resulting *electrical* length is out of specification, then its total *physical* length shall be scaled accordingly to adjust this error.

The test frequency f_T is chosen to be a typical mid-band frequency in the spectrum of long range SHDSL systems. The length is chosen to be a typical maximum value that can be handled correctly by the SHDSL transceiver under test. This value is bit rate dependent; the higher the payload bit rate, the lower is the insertion loss that can be handled in practice.

Table B.1/G.991.2 – Values of the electrical length Y of the SHDSL noise test loops, when testing SHDSL at noise model A

Payload bit rate [kbit/s]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L7 [m]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L6 [m]
384	150	43.0	<3	4106	5563	5568	11 064	4698	115	40.5	3165
512	150	37.0	<3	3535	4787	4789	9387	3996	115	35.0	2646
768	150	29.0	<3	2773	3747	3753	7153	3062	275	34.5	1904
1024	150	25.5	<3	2439	3285	3291	6174	2668	275	30.0	1547
1280	150	22.0	<3	2105	2829	2837	5193	2266	275	26.0	1284
1536	150	19.0	<3	1820	2453	2455	4357	1900	250	21.5	1052
2048 (s)	200	17.5	<3	1558	2046	2052	3285	1550	250	18.5	748
2304 (s)	200	15.5	<3	1381	1815	1820	2789	1331	250	16.5	583
2048 (a)	250	21.0	<3	1743	2264	2272	3618	1726	250	21.0	1001
2304 (a)	250	18.0	<3	1494	1927	1937	2915	1402	250	18.0	702
NOTE – The electrical length Y (insertion loss at specified frequency f_T) is mandatory, the (estimated) physical lengths L1-L7 are informative. (s) those electrical lengths apply to the symmetric PSD. (a) those electrical lengths apply to the asymmetric PSD.											

Table B.2/G.991.2 – Values of the electrical length Y of the SHDSL noise test loops, when testing SHDSL at noise model B, C, or D

Payload bit rate [kbit/s]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L7 [m]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L6 [m]
384	150	50.0	<3	4773	6471	6477	13 021	5508	115	47.5	3859
512	150	44.0	<3	4202	5692	5698	11 344	4814	115	41.5	3261
768	150	35.5	<3	3392	4592	4596	8970	3815	275	42.0	2536
1024	150	32.0	<3	3058	4135	4141	7990	3403	275	38.0	2223
1280	150	28.5	<3	2725	3678	3684	7011	3006	275	33.5	1816
1536	150	25.5	<3	2439	3285	3291	6174	2673	250	29.0	1680
2048 (s)	200	24.0	<3	2135	2812	2820	4886	2271	250	25.5	1426
2304 (s)	200	21.5	<3	1913	2509	2518	4257	2010	250	23.0	1208

Table B.2/G.991.2 – Values of the electrical length Y of the SHDSL noise test loops, when testing SHDSL at noise model B, C, or D

Payload bit rate [kbit/s]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L7 [m]	f_T [kHz]	Y [dB] @f_T, @135 Ω	L6 [m]
2048 (a)	250	28.0	<3	2323	3030	3034	5189	2389	250	28.0	1607
2304 (a)	250	25.0	<3	2075	2699	2705	4514	2102	250	25.0	1387
NOTE – The electrical length Y (insertion loss at specified frequency f_T) is mandatory, the (estimated) physical lengths L1-L7 are informative. (s) those electrical lengths apply to the symmetric PSD. (a) those electrical lengths apply to the asymmetric PSD.											

B.3 Performance testing

The purpose of transmission performance tests is to stress SHDSL transceivers in a way that is representative to a high penetration of systems scenario in operational access networks. This high penetration approach enables operators to define deployment rules that apply to most operational situations. It means also that in individual operational cases, characterized by lower noise levels and/or insertion loss values, the SHDSL system under test may perform better than tested.

The design impedance R_V is 135 Ω. All spectra are representing single sided power spectral densities (PSD).

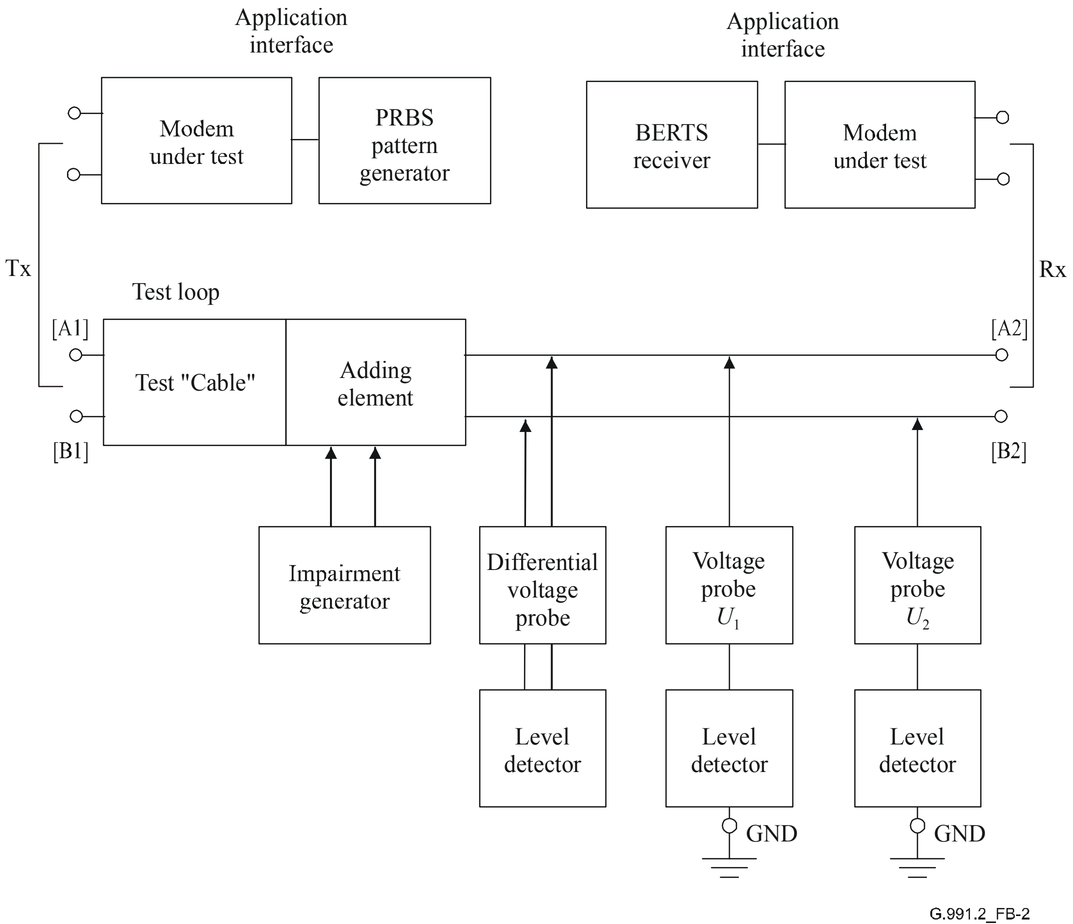
B.3.1 Test procedure

The purpose of this clause is to provide an unambiguous specification of the test set-up, the insertion path and the way signal and noise levels are defined. The tests are focused on the noise margin, with respect to the crosstalk noise or impulse noise levels when SHDSL signals under test are attenuated by standard test-loops and interfered with standard crosstalk noise or impulse noise. This noise margin indicates what increase of crosstalk noise or impulse noise level is allowed under specific operational conditions to ensure sufficient transmission quality.

B.3.2 Test set-up definition

Figure B.2 illustrates the functional description of the test set-up. It includes:

- A bit error ratio test set (BERTS) applies a $2^{15} – 1$ pseudo-random bit sequence (PRBS) test signal to the transmitter in the direction under test at the bit rate required. The transmitter in the opposing direction shall be fed with a similar PRBS signal, although the reconstructed signal in this path need not be monitored.
- The test loops, as specified in B.2.
- An adding element to add the (common mode and differential mode) impairment noise (a mix of random, impulsive and harmonic noise), as specified in B.3.5.
- An impairment generator, as specified in B.3.5, to generate both the differential mode and common mode impairment noise, that are fed to the adding element.
- A high impedance, and well-balanced differential voltage probe (e.g., better than 60 dB across the whole band of the SHDSL system under test) connected with level detectors such as a spectrum analyser or a true RMS voltmeter.
- A high impedance, and well-balanced common mode voltage probe (e.g., better than 60 dB across the whole band of the SHDSL system under test) connected with level detectors such as a spectrum analyser or a true RMS voltmeter.



NOTE – To allow test reproducibility, the testing equipment and the Termination Units (STU-C and STU-R) should refer to an artificial earth. If the Termination Units have no earth terminal, the test should be performed while the Termination Units are placed on a metal plate (of sufficient large size) connected to earth.

Figure B.2/G.991.2 – Functional description of the set-up of the performance tests

The two-port characteristics (transfer function, impedance) of the test-loop, as specified in B.2, are defined between port TX (node pairs A1, B1) and port RX (node pair A2, B2). The consequence is that the two-port characteristics of the test "cable" in Figure B.2 must be properly adjusted to take full account of non-zero insertion loss and non-infinite shunt impedance of the adding element and impairment generator. This is to ensure that the insertion of the generated impairment signals does not appreciably load the line.

The balance about earth, observed at port TX, at port RX, and at the tips of the voltage probe shall exhibit a value that is 10 dB greater than the transceiver under test. This is to ensure that the impairment generator and monitor function do not appreciably deteriorate the balance about earth of the transceiver under test.

The signal flow through the test set-up is from port TX to port RX, which means that measuring upstream and downstream performance requires an interchange of transceiver position and test "cable" ends.

The received signal level at port RX is the level, measured between node A2 and B2, when port TX as well as port RX are terminated with the SHDSL transceivers under test. The impairment generator is switched off during this measurement.

Test Loop #1, as specified in B.2, shall always be used for calibrating and verifying the correct settings of generators G1-G7, as specified in B.3.5, when performing performance tests.

The transmitted signal level at port TX is the level, measured between node A1 and B1, under the same conditions.

The impairment noise shall be a mix of random, impulsive and harmonic noise, as defined in B.3.5. The level that is specified in B.3.5 is the level at port RX, measured between node A2 and B2 (and includes both differential mode and common mode impairments), while port TX as well as port RX are terminated with the design impedance R_V. These impedances shall be passive when the transceiver impedance in the switched-off mode is different from this value.

NOTE – The injected noise is intended to match the theoretical noise PSD when the transceiver under test is connected to the loop. On loop #2 and #3 for payload rates of 1024 kbit/s and below, it has been found that impedance mismatch could generate an increased noise PSD at low frequencies. One method of compensation is to modify the factor, Δ, defined in A.3.1.4, by replacing the theoretical noise, *N(f)*, in step 3 of A.3.1.4 with the noise PSD measured when connected to the loop under test. A second method is to place a passive circuit, consisting of a resistor R in parallel with a capacitor C, in series with each wire of the noise generator output pair. The RC values of R = 1.2 Kohms and C = 1 μF are suggested and should be adjusted for each noise generator such that the injected noise matches the theoretical noise PSD. A third method is to calibrate the noise generator waveform into the loop under test such that when connected to the loop under test, the theoretical noise waveform is present at the transceiver terminals.

B.3.3 Signal and noise level definitions

The signal and noise levels are probed with a well-balanced differential voltage probe, and the differential impedance between the tips of the probe shall be higher than the shunt impedance of 100 kΩ in parallel with 10 pF. Figure B.2 shows the probe position when measuring the RX signal level at the STU-C or STU-R receiver. Measuring the TX signal level requires the connection of the tips to node pair [A1, B1].

The various PSDs of signals and noises specified in this Recommendation are defined at the TX or RX side of the set-up. The levels are defined when the set-up is terminated, as described above, with design impedance R_V or with transceivers under test.

Probing an rms-voltage U_{rms} [V] in this set-up, over the full signal band, means a power level of P[dBm] that equals:

$$P = 10 \times \log_{10}\left(\frac{U_{rms}^2}{R_V} \times 1000\right) \text{ [dBm]}$$

Probing an rms-voltage U_{rms} [V] in this set-up, within a small frequency band of Δf (in Hertz), corresponds to an average spectral density level of P[dBm/Hz] within that filtered band that equals:

$$P = 10 \times \log_{10}\left(\frac{U_{rms}^2}{R_V} \times \frac{1000}{\Delta f}\right) \text{[dBm/Hz]}$$

The bandwidth Δf identifies the noise bandwidth of the filter, and not the –3 dB bandwidth.

B.3.3.1 Noise injection network

B.3.3.1.1 Differential mode injection

The noise injector for differential mode noise (which is the portion of the Adding Element shown in Figure B.2 that is used to couple differential impairments to the test cable) is a two-port network in nature, and may have additional ports connected to the impairment generator. The Norton equivalent circuit diagram is shown in Figure B.2a. The current source I_x is controlled by the impairment generator. The parasitic shunt impedance Z_{inj} shall have a value of $|Z_{inj}| > 4$ kΩ in the frequency range from 100 Hz to 2 MHz.

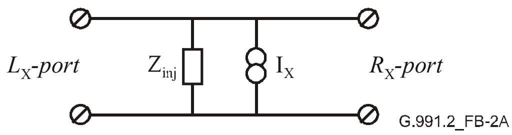


Figure B.2a/G.991.2 – Norton equivalent circuit diagram for differential mode noise injection

B.3.3.1.2 Common mode injection

The specification of this injection network is for further study.

B.3.3.2 Noise levels calibration

B.3.3.2.1 Differential mode noise calibration

The differential mode noise injection is calibrated using the configuration shown in Figure B.2b. During calibration the RX side of the noise injector is terminated by the design impedance R_V (= 135 Ω) and the LX (Test Loop interface) side of the noise injector is terminated by an impedance Z_{LX}. The noise levels given in B.3.5 specify the PSD dissipated in R_V on the RX side when Z_{LX} on the LX side is equal to the calibration impedance Z_{cal}. The impedance Z_{cal} is defined in Figure B.2c.

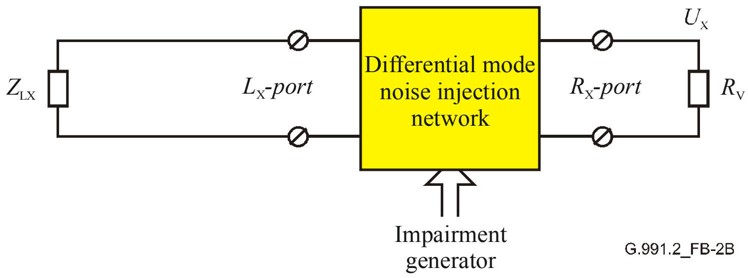


Figure B.2b/G.991.2 – Configuration for noise level calibration

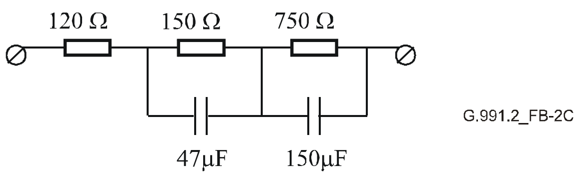


Figure B.2c/G.991.2 – Calibration impedance Z_{cal}

The impedance Z_{LX} on the LX side of the noise injection circuit is equal to the calibration impedance Z_{cal} as given in Figure B.2c. The PSD dissipated in the impedance R_V shall be equal to the differential noise PSD $P_{xn}(f)$ defined in B.3.5.1.

NOTE – This is theoretically equivalent to the following: For an arbitrary value of the impedance Z_{LX}, the PSD dissipated in R_V is equal to:

$$P_{cal}(f) = G(f, Z_{LX}) P_{xn}(f)$$

where $G(f, Z_{LX})$ is the impedance dependent correction factor, which is specified as:

$$G(f, Z_{LX}) = \left| \frac{\frac{1}{Z_{LX}} + \frac{1}{Z_{inj}} + \frac{1}{R_v}}{\frac{1}{Z_{cal}} + \frac{1}{Z_{inj}} + \frac{1}{R_v}} \right|^2$$

where Z_{cal} is the calibration impedance given in Figure B.2c, Z_{inj} is the Norton equivalent impedance of the noise injection circuit (see Figure B.2a), and R_V = 135 Ω is the SHDSL design impedance.

The noise generator gain settings determined during calibration shall be used during performance testing. During performance testing the noise injection circuit will be configured as shown in Figure B.2. Because the loop impedance and the impedance of the modem under test may differ from the impedance's Z_{LX} and R_V used during calibration, the voltage over the RX port of the modem may differ from the voltage U_X observed during calibration.

B.3.3.2.2 Common mode noise calibration

This calibration method is for further study.

B.3.4 Performance test procedure

The test performance of the SHDSL transceiver shall be such that the bit error ratio (BER) on the disturbed system is less than 10^{-7}, while transmitting a pseudo-random bit sequence. The BER should be measured after at least 10^9 bits have been transmitted.

The tests are carried out with a margin which indicates what increase of noise is allowed to ensure sufficient transmission quality. Network operators may calculate their own margins for planning purposes based on a knowledge of the relationship between this standard test set and their network characteristics.

A test sequence as specified in Table B.3 shall be concluded. The test loops referred to are specified in Figure B.1. The test loops are characterized by the insertion loss Y and/or the cable length L, which depend on the data rate to be transported and have to be scaled adequately.

In Table B.3, upstream and downstream only determine the topology of the test loop. The STU-C must pass all tests 1 through 12. The STU-R must pass all tests 1 through 12.

A test is defined as the measurement of a given BER associated with a single test path, direction, test noise, rate and margin. The ensemble of tests associated with a particular value of N in Table B.3 is defined as a test set.

Table B.3/G.991.2 – Test sequence for performance testing

N	Test path	Direction (Note 6)	Comments
1	#1 (Note 1)	Upstream	Y = 0 dB; Test noise A (Notes 5, 7)
2	#2	Upstream	Y = Y1 (Note 2); Test noise A, C and D (Notes 7, 8)
3	#3	Upstream	Y = Y1; Test noise D (Notes 5, 7, 8)
4	#4	Downstream	Y = Y1; Test noise A and C (Notes 5, 7, 8)
5	#5	Upstream	Y = Y1; Test noise B (Notes 5, 7, 8)
6	#6	Downstream	Y = Y1; Test noise A and C (Notes 5, 7, 8)
7	#7	Downstream	Y = Y1; Test noise A, B, C and D (Notes 5, 7, 8)
8			Common mode rejection test (Note 4)
9	(Note 3)	(Note 3)	Y = Y2; Test noise is the noise corresponding to the test with the highest BER in test sets 1 through 7 (Note 7)
10	(Note 3)	(Note 3)	Y = Y3; No added impairment; Worst path of tests 1 to 7; BER < 10^{-8}
11	#2	Upstream	Y = Y1; Impulse test as described in B.3.5.3.7
12	As <TBD>	<TBD>	Micro-interruption test as described in 12.1

Table B.3/G.991.2 – Test sequence for performance testing

NOTE 1 – Test Path = #1 means that the path under test shall be connected with test loop #1 as defined in Figure B.1.

NOTE 2 – Y1 = Y dB (as specified in Table B.2 for noise models B, C and D and in Table B.1 for noise model A), Y2 = Y1 – 10 dB, Y3 = Y1 + 3 dB.

NOTE 3 – The tests (for any data rate) are carried out on the loop that gives the highest BER (for that data rate) in test sets 1 through 7, when the test noise is increased by 6 dB. If no errors in 109 bits are recorded for all the tests in test sets 1 through 7, then loop #3 upstream is used for this test set by default.

NOTE 4 – The measuring arrangement for this test is specified in ITU-T Rec. O.9 [B8].

NOTE 5 – Only tested for lowest and highest data rate in Table B.1 or Table B.2 (that the equipment supports) and for asymmetric PSDs when supported.

NOTE 6 – Upstream means that the unit under test is connected to the STU-C end of the test loop and downstream means that the unit under test is connected to the STU-R end of the test loop. For example, test set 5 for an STU-C would connect the STU-C under test to the STU-C end of the loop as shown in Figure B.1 and apply noise model X.C.B to the STU-C end of the loop. The same test for an STU-R would connect the STU-R under test to the STU-C end of the loop as shown in Figure B.1 and apply noise model X.R.B to the STU-C end of the loop.

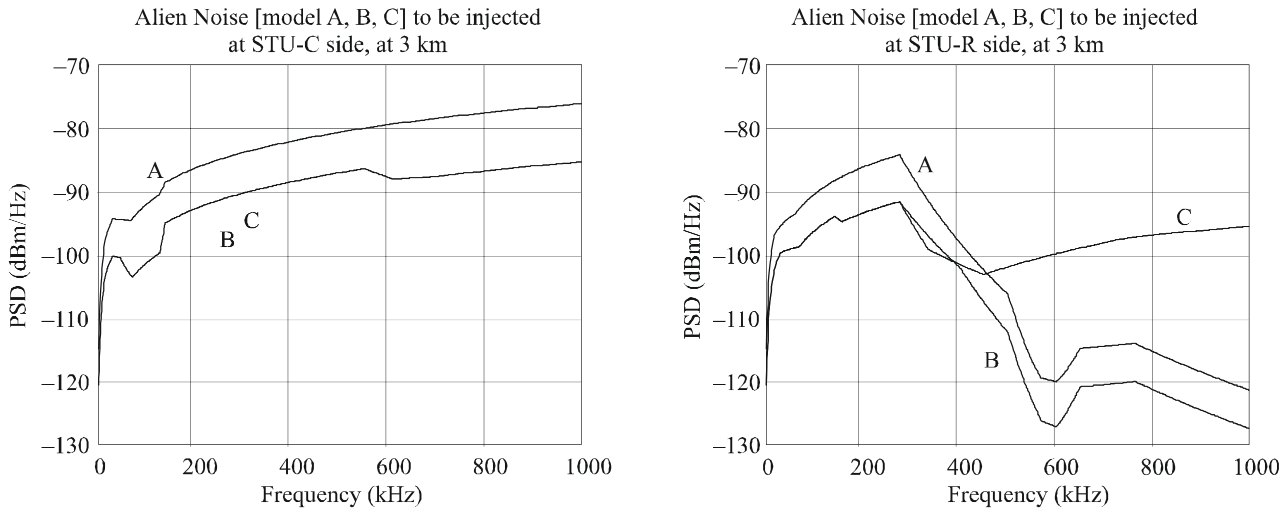
NOTE 7 – The BER shall be less than 10^{-7} when the test noise is increased by 6 dB (this is equivalent to 6 dB of margin).

NOTE 8 – In order to reduce the number of noise shapes used, a mandatory noise shape substitution rule is given in B.3.5.5.

NOTE 9 – To test the *M*-pair mode, while one path is under test, the other path(s) must be connected to loop(s). The characteristics of the other loop(s) must not be worse than the ones of the path under test. Furthermore, the differential delay between the path under test and the path(s) connected to the second loop should not exceed the value of the differential delay buffer specified in 7.1.6.

B.3.5 Impairment generator

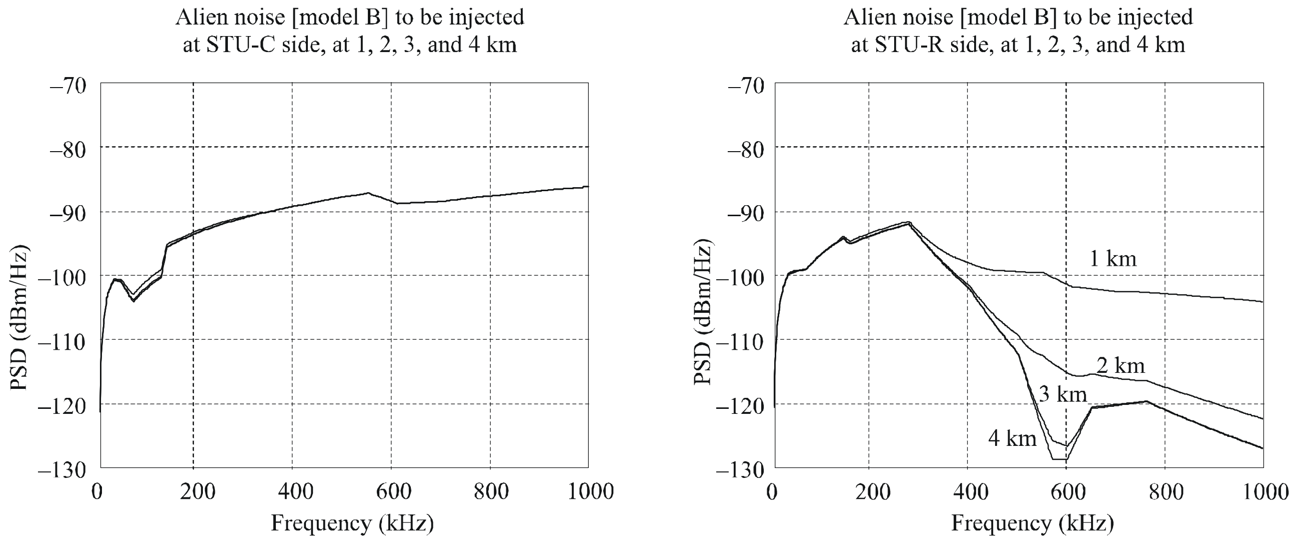
The noise that the impairment generator injects into the test set-up is frequency dependent, is dependent on the length of the test loop and is also different for downstream performance tests and upstream performance tests. Figure B.3 illustrates this for the ***alien*** noise (other than the SHDSL modem under test), as described in B.3.5.4.1, for the case that the length of test loop #1 is fixed at 3 km, using the crosstalk models described in B.3.5.2. Figure B.4 illustrates this for various loop lengths for the case that the ***alien*** noise of model "B" is applied. These figures are restricted to alien noise only. The self noise (of SHDSL) shall be combined with this alien noise.



NOTE – This is the noise resulting from three of the four noise models for SHDSL in the case that the length of test loop #2 is fixed at 3 km.

G.991.2_FB-3

Figure B.3/G.991.2 – Examples of alien noise spectra that are to be injected into the test set-up, while testing SHDSL systems



NOTE – This is the alien noise, resulting from noise model B for SHDSL, in the case that the length of test loop #2 varies from 1 km to 4 km. This demonstrates that the test noise is length dependent, to represent the FEXT in real access network cables.

G.991.2_FB-4

Figure B.4/G.991.2 – Examples of alien noise spectra that are to be injected into the test set-up, while testing SHDSL systems

The definition of the impairment noise for SHDSL performance tests is very complex and for the purposes of this Recommendation it has been broken down into smaller, more easily specified components. These separate, and uncorrelated, impairment "generators" may therefore be isolated and summed to form the impairment generator for the SHDSL system under test. The detailed specifications for the components of the noise model(s) are given in this clause, together with a brief explanation.

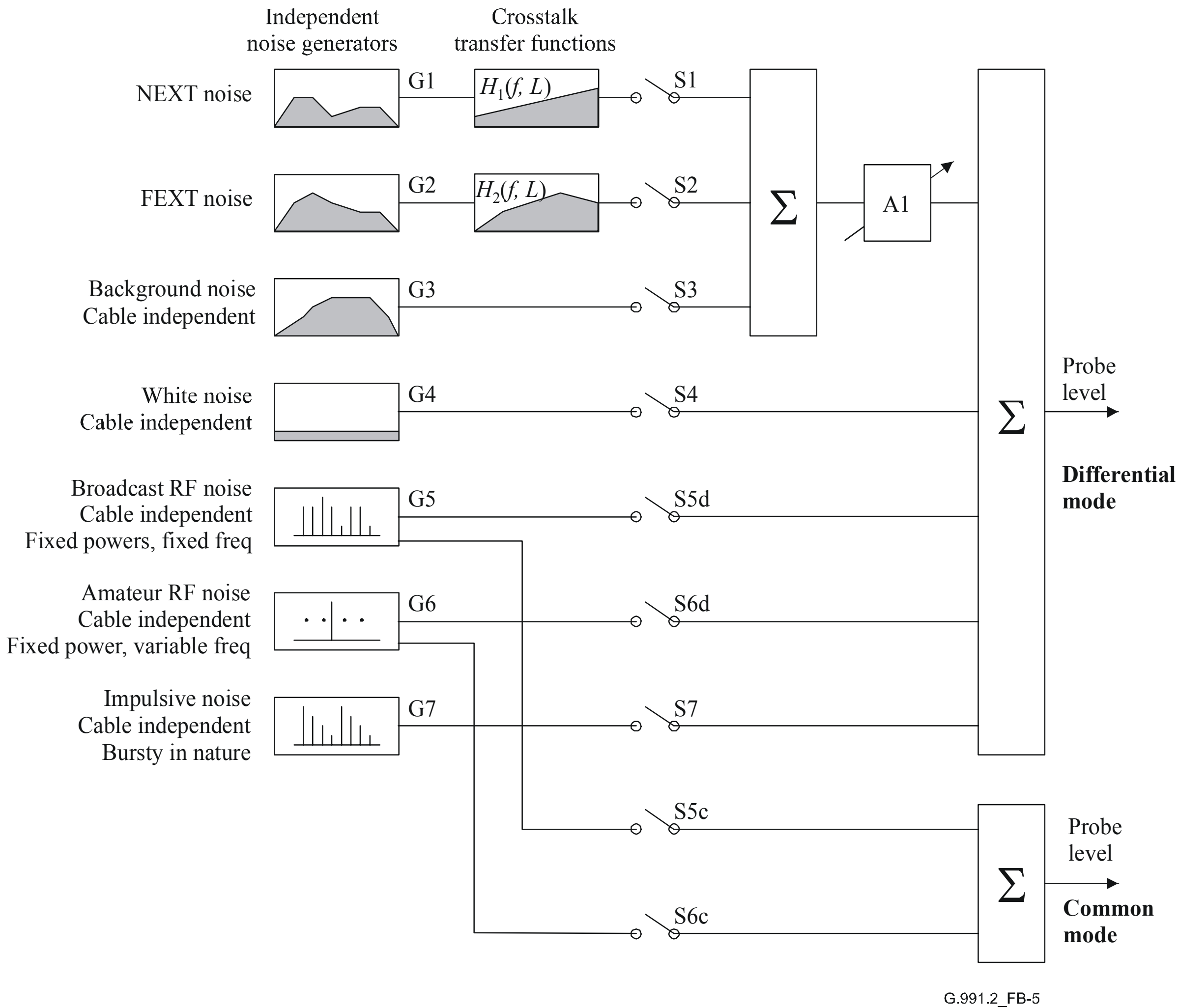
B.3.5.1 Functional description

Figure B.5 defines a functional diagram of the composite impairment noise. It defines a functional description of the combined impairment noise as it must be probed at the receiver input of the SHDSL transceiver under test. The probing is described in B.3.3.

The functional diagram has the following elements:

- The seven impairment "generators" G1 to G7 generate noise as defined in B.3.5.3.1 to B.3.5.3.7. Their noise characteristics are independent from the test loops and bit rates.
- The transfer function $H_1(f, L)$ models the length and frequency dependency of the NEXT impairment, as specified in B.3.5.3.1. The transfer function is independent of the test loops, but changes with the electrical length of the test loop. Its transfer function changes with the frequency f, roughly according to $f^{0.75}$.
- The transfer function $H_2(f, L)$ models the length and frequency dependency of the FEXT impairment, as specified in B.3.5.3.2. Its transfer function is independent of the test loops, but changes with the electrical length of the test loop. Its transfer function changes with the frequency f, roughly according to f times the cable transfer function.
- Switches S1-S7 determine whether or not a specific impairment generator contributes to the total impairment during a test.
- Amplifier A1 models the property to increase the level of some generators simultaneously to perform the noise margin tests. A value of x dB means a frequency independent increase of the level by x dB over the full band of the SHDSL system under test, from f_L to f_H. Unless otherwise specified, its gain is fixed at 0 dB.

In a practical implementation of the test set-up, there is no need to give access to any of the internal signals of the diagram in Figure B.5. These functional blocks may be incorporated with the test loop and the adding element as one integrated construction.



NOTE 1 – Generator G7 is the only one that is symbolically shown in the time domain.
NOTE 2 – The precise definition of impulse noise margin is for further study.

Figure B.5/G.991.2 – Functional diagram of the composition of the impairment noise

This functional diagram will be used for impairment tests in downstream and upstream direction. Several scenarios have been identified to be applied to SHDSL testing. These scenarios are intended to be representative of the impairments found in metallic access networks.

Each scenario (or noise model) results in a length-dependent and test loop-dependent PSD description of noise. Each noise model is subdivided into two parts: one to be injected at the STU-C side, and another to be injected at the STU-R side of the SHDSL modem link under test. Therefore, seven individual impairment generators G1 to G7 can represent different values for each noise model they are used in. Specifically, G1 and G2 are dependent on which unit, STU-R or STU-C, is under test.

Generators G1-G4 represent crosstalk noise. The spectral power $P_{xn}(f)$ for crosstalk noise is characterized by the sum:

$$P_{xn}(f) = |A1|^2 \times \{ |H_1(f, L)|^2 \times P_{G1}(f) + |H_2(f, L)|^2 \times P_{G2}(f) + P_{G3}(f) \} + P_{G4}(f)$$

Each component of this sum is specified in the following clauses. Only the noise generators that are active during testing should be included during calibration. This combined impairment noise is applied to the receiver under test, at either the STU-C (for upstream) or STU-R (for downstream) ends of the test-loop.

Generators G5 and G6 represent ingress noise.

B.3.5.2 Cable crosstalk models

The purpose of the cable crosstalk models is to model both the length and frequency dependency of crosstalk measured in real cables. These crosstalk transfer functions adjust the level of the noise generators in Figure B.5 when the electrical length of the test loops is changed. The frequency and length dependency of these functions is in accordance with observations from real cables. The specification is based on the following constants, parameters and functions:

- Variable f identifies the frequency in Hz.
- Constant f_0 identifies a chosen reference frequency, which was set to 1 MHz.
- Variable L identifies the physical length of the actual test loop in metres. This physical length is calculated from the cable models in Appendix II from the specified electrical length. Values are summarized in Tables B.1 and B.2 for each combination of payload bit rate, noise model, and test loop.
- Constant L_0 identifies a chosen reference length, which was set to 1 km.
- Function $s_{T0}(f, L)$ represents the frequency and length dependent amplitude of the insertion loss of the actual test loop terminated into 135 Ω.
- Constant K_{xn} identifies an empirically obtained number that scales the NEXT transfer function $H_1(f, L)$. The resulting transfer function represents a power summed crosstalk model of the NEXT as it was observed in a test cable. Although several disturbers and wire pairs were used, this function $H_1(f, L)$ is scaled down as if it originates from a single disturber in a single wire pair.
- Constant K_{xf} identifies an empirically obtained number that scales the FEXT transfer function $H_2(f, L)$. The resulting transfer function represents a power summed crosstalk model of the FEXT as it was observed in a test cable. Although several disturbers and wire pairs were used, this function $H_2(f, L)$ is scaled down as if it originates from a single disturber in a single wire pair.

The transfer functions in Table B.4 shall be used as crosstalk transfer functions in the impairment generator.

Table B.4/G.991.2 – Definition of the crosstalk transfer functions

$H_1(f,L) = K_{xn} \times \left(\frac{f}{f_0}\right)^{0.75} \times \sqrt{1-\lvert s_{T0}(f,\ L)\rvert^4}$ $H_2(f,L) = K_{xf} \times \left(\frac{f}{f_0}\right) \times \sqrt{\frac{L}{L_0}} \times \lvert S_{T0}(f,L)\rvert$
$K_{xn} = 10^{(-50/20)} \approx 0.0032$, $f_0 = 1$ MHz $K_{xf} = 10^{(-45/20)} \approx 0.0056$, $L_0 = 1$ km $S_{T0}(f,L)$ = test loop insertion loss

B.3.5.3 Individual impairment generators

B.3.5.3.1 Equivalent NEXT disturbance generator [G1.xx]

The NEXT noise generator represents the equivalent disturbance of all impairment that is identified as crosstalk noise from a predominantly near end origin. This noise, filtered by the NEXT crosstalk coupling function of B.3.5.2, will represent the contribution of all NEXT to the composite impairment noise of the test.

The PSD of this noise generator is one of the PSD profiles, as specified in B.3.5.4. For testing upstream and downstream performance, different PSD profiles shall be used, as specified below.

G1.C.# = X.C.#

G1.R.# = X.R.#

The symbols in this expression, refer to the following:

- Symbol "#" is a placeholder for noise model "A", "B" , "C" or "D".
- Symbols "X.C.#" and "X.R.#" refer to the crosstalk profiles, as defined in B.3.5.4.

This PSD is not related to the cable because the cable portion is modelled separately as transfer function $H_1(f, L)$, as specified in B.2.2.

The noise of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in B.3.5.4.2.

B.3.5.3.2 Equivalent FEXT disturbance generator [G2.xx]

The FEXT noise generator represents the equivalent disturbance of all impairment that is identified as crosstalk noise from a predominantly far end origin. This noise, filtered by the FEXT crosstalk coupling function of B.3.5.2, will represent the contribution of all FEXT to the composite impairment noise of the test.

The PSD of this noise generator is one of the PSD profiles, as specified in B.3.5.4.1. For testing upstream and downstream performance, different PSD profiles shall be used, as specified below.

G2.C.# = X.R.#

G2.R.# = X.C.#

The symbols in this expression, refer to the following:

- Symbol "#" is a placeholder for noise model "A", "B", "C" or "D".
- Symbols "X.C.#" and "X.R.#" refer to the crosstalk profiles, as defined in B.3.5.4.

This PSD is not related to the cable because the cable portion is modelled separately as transfer function $H_2(f, L)$, as specified in B.2.2.

The noise of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in B.3.5.4.2.

B.3.5.3.3 Background noise generator [G3]

The background noise generator is inactive and set to zero.

B.3.5.3.4 White noise generator [G4]

The white noise generator has a fixed, frequency independent value, and is set to a level between –140 and –120 dBm/Hz, into 135 Ω. The output signal of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in B.3.5.4.2.

B.3.5.3.5 Broadcast RF noise generator [G5]

NOTE 1 – Work on a specification dealing with generic RFI testing methods is ongoing. It is expected that a future version of this Recommendation will contain a complete RFI testing specification, which will be mandatory. This clause is currently for information only.

The broadcast RF noise generator represents the discrete-tone line interference caused by amplitude modulated broadcast transmissions in the SW, MW and LW bands, which ingress into the cable. These interference sources have more temporal stability than the amateur (ham) interference (see B.3.5.3.6) because their carriers are not suppressed. Ingress causes differential mode as well as common mode interference.

The ingress noise signal for differential mode impairment (or common mode impairment) is a superposition of random modulated carriers (AM). The total voltage $U(t)$ of this signal is defined as:

$$U(t) = \mathbf{\Sigma_k}\ U_k \times cos(2\pi \cdot f_k \times t + \varphi_k) \times (1 + m \times \alpha_k(t))$$

The individual components of this ingress noise signal $U(t)$ are defined as follows:

– $\boldsymbol{U_k}$ – The voltage U_k of each individual carrier should be as specified in Table B.5 as power level P (dBm) into a resistive load R, equal to the design impedance R_V = 135 Ω. Note that spectrum analysers will detect levels that are slightly higher than the values specified in Table B.5 when their resolution bandwidths are set to 10 kHz or more, since they will detect the modulation power as well.

– $\boldsymbol{f_k}$ – The frequency f_k of each individual carrier should be as specified in Table B.5. The frequency values in Table B.5 do not represent actual broadcast frequencies but are chosen such that they cover the frequency range that is relevant for SHDSL modems. Note that the harmonic relation between the carriers in Table B.5 is minimal.

– $\boldsymbol{\varphi_k}$ – The phase offset φ_k of each individual carrier shall have a random value that is uncorrelated with the phase offset of every other carrier in the ingress noise signal.

– $\boldsymbol{m}$ – The modulation depth m of each individually modulated carrier shall be m = 0.32, to enable a modulation index of at least 80 % during the peak levels of the modulation signal $m \times \alpha_k(t)$.

– $\boldsymbol{\alpha_k(t)}$ – The normalized modulation noise $\alpha_k(t)$ of each individually modulated carrier shall be random in nature, shall be Gaussian distributed in nature, shall have an rms value of α_{rms} = 1, shall have a crest factor of 2.5 or more, and shall be uncorrelated with the modulation noise of each other modulated carrier in the ingress noise signal.

– $\boldsymbol{\Delta b}$ – The modulation width Δb of each modulated carrier shall be at least 2 × 5 kHz. This is equivalent to creating $\alpha_k(t)$ from white noise, filtered by a low-pass filter with a cut-off frequency at $\Delta b/2$ = 5 kHz. This modulation width covers the full modulation band used by AM broadcast stations.

NOTE 2 – The precise specification of the spectral shape requirements of the modulation signal is for further study.

Table B.5/G.991.2 – Average minimum RFI noise power versus frequency

frequency (kHz)	153	207	270	531	603	711	801	909	981	1296
power (dBm)	–70	–44	–70	–70	–49	–70	–70	–44	–70	–49

B.3.5.3.6 Amateur RF noise generator [G6]

The amateur radio noise generator is identical to the broadcast RF noise generator with different frequency and power values. These values are for further study.

B.3.5.3.7 Impulse noise generator [G7]

A test with this noise generator is required to prove the burst noise immunity of the SHDSL transceiver. This immunity shall be demonstrated on short and long loops and noise to model crosstalk and RFI.

B.3.5.4 Profiles of the individual impairment generators

Crosstalk noise represents all impairment that originates from systems connected to adjacent wire pairs that are bundled in the same cable. Their wires are coupled to the wires of the xDSL system under test, causing this spectrum of crosstalk noise to vary with the electrical length of the test loop.

To simplify matters, the definition of crosstalk noise has been broken down into smaller, more easily specified components. The two generators G1 and G2 represent the "equivalent disturbance". Their noise level originate from a mixture of many disturbers in a real scenario, as if all disturbers are collocated at the ends of the test loops.

This equivalent disturbance, filtered by the NEXT and FEXT coupling functions, will represent the crosstalk noise that is to be injected in the test set-up. This approach has isolated their definition from the NEXT and FEXT coupling functions of the cable. The noise generated by these two equivalent disturbers is specified in this clause in the frequency domain as well as in the time domain.

The frequency domain characteristics of each generator G1 and G2 is defined by a spectral profile, so each noise model has its own pair of spectral profiles.

- The profiles X.C.# in this clause describe the total equivalent disturbance of a technology mix that is virtually colocated at the STU-C end of the test loop. This noise is represented by equivalent disturbance generator G1, when stressing upstream signals, and by equivalent disturbance generator G2 when stressing downstream signals.
- The profiles X.R.# in this clause describe the total equivalent disturbance of a technology mix that is virtually colocated at the STU-R end of the test loop. This noise is represented by equivalent disturbance generator G2, when stressing upstream signals, and by equivalent disturbance generator G1 when stressing downstream signals.

Note that the PSD levels of equivalent disturbance generator G1 and G2 are interchanged when changing from upstream testing to downstream testing.

B.3.5.4.1 Frequency domain profiles for SHDSL

This subclause specifies the PSD profiles X.R.# and X.C.# that apply for the equivalent disturbers G1 and G2 when testing SHDSL systems. In this nomenclature, "#" is used as a placeholder for noise model "A", "B" ,"C" and "D".

Four noise models have been defined for SHDSL:

- **Type "A" models** are intended to represent a high penetration scenario where the SHDSL system under test is placed in a distribution cable (up to hundreds of wire pairs) that is filled with many other (potentially incompatible) transmission systems.
- **Type "B" models** are intended to represent a medium penetration scenario where the SHDSL system under test is placed in a distribution cable (up to tens of wire pairs) that is filled with many other (potentially incompatible) transmission systems.
- **Type "C" models** are intended to represent a legacy scenario that accounts for systems such as ISDN-PRI (HDB3), in addition to the medium penetration scenario of model "B".
- **Type "D" models** are intended as reference scenario to demonstrate the difference between a cable filled with SHDSL only, or filled with a mixture of SHDSL techniques.

The PSD profiles for each noise model are build up by a weighed sum of two individually defined profiles: self and alien crosstalk profiles.

X.C.# = (XS.C.# ♦ XA.C.#)

X.R.# = (XS.R.# ♦ XA.R.#)

The symbols in this expression refer to the following:

- Symbols "#" is used as a placeholder for noise model "A", "B", "C" or "D".
- Symbols "XS.C.#" and "XS.R.#" refer to the self crosstalk profiles, as defined in B.3.5.4.1.1.
- Symbol "XA.C.#" and "XA.R.#" refer to the alien crosstalk profiles, as defined in B.3.5.4.1.2.
- Symbol "♦" refers to the crosstalk sum of two PSDs, defined as $P_X = \left(P_{XS}{}^{K_n} + P_{XA}{}^{K_n}\right)^{1/K_n}$ where P denotes the PSDs in W/Hz, and K_n = 1/0.6.

These profiles shall be met for all frequencies between 1 kHz to 1 MHz.

B.3.5.4.1.1 Self crosstalk profiles

The noise profiles XS.C.# and XS.R.#, representing the equivalent disturbance of self crosstalk, are specific to the PSD parameters of the SHDSL system under test, defined by the specific payload, symmetry and power-back-off features. For compliance with the requirements of this Recommendation, the appropriate nominal PSD from B.4 shall be used.

For testing SHDSL, four noise models for self crosstalk have been defined. The STU-R and STU-C profiles are specified in Table B.6.

In this nomenclature, "#" is a placeholder for model "A", "B" ,"C" or "D". "SHDSL.dn" is the signal spectrum that SHDSL transmits in downstream direction, and "SHDSL.up" in upstream direction.

Table B.6/G.991.2 – Definition of the self crosstalk for SHDSL testing

	Model A (XS.#.A)	**Model B (XS.#.B)**	**Model C (XS.#.C)**	**Model D (XS.#.D)**
XS.C.#:	"SHDSL.dn" + 11.7 dB	"SHDSL.dn" + 7.1 dB	"SHDSL.dn" + 7.1 dB	"SHDSL.dn" + 10.1 dB
XS.R.#:	"SHDSL.up" + 11.7 dB	"SHDSL.up" + 7.1 dB	"SHDSL.up"+ 7.1 dB	"SHDSL.up" + 10.1 dB
NOTE – The different noise models use different Gain factors.				

B.3.5.4.1.2 Alien crosstalk profiles

The noise profiles XA.C.# and XA.R.#, representing the equivalent disturbance of alien crosstalk, are implementation specific for the SHDSL system under test. For testing SHDSL, four noise models for alien crosstalk have been defined. The STU-C profiles are specified in Table B.7 and the STU-R profiles in Table B.8. Each PSD profile originates from a mix of disturbers. The alien noise in model D is made inactive, to achieve one pure self crosstalk scenario.

Table B.7/G.991.2 – Break frequencies of the "XA.C.#" PSD profiles that specify the equivalent disturbance spectra of alien disturbers

XA.C.A [Hz]	135 Ω [dBm/Hz]	XA.C.B [Hz]	135 Ω [dBm/Hz]	XA.C.C [Hz]	135 Ω [dBm/Hz]	XA.C.D [Hz]	135 Ω [dBm/Hz]
1	–20.0	1	–25.7	1	–25.7		
15 k	–20.0	15 k	–25.7	15 k	–25.7		
30 k	–21.5	30 k	–27.4	30 k	–27.4	ALL	–∞
67 k	–27.0	45 k	–30.3	45 k	–30.3		
125 k	–27.0	70 k	–36.3	70 k	–36.3		
138 k	–25.7	127 k	–36.3	127 k	–36.3		
400 k	–26.1	138 k	–32.1	138 k	–32.1		
1104 k	–26.1	400 k	–32.5	400 k	–32.5		
2.5 M	–66.2	550 k	–32.5	550 k	–32.5		
4.55 M	–96.5	610 k	–34.8	610 k	–34.8		
30 M	–96.5	700 k	–35.4	700 k	–35.3		
		1104 k	–35.4	1104 k	–35.3		
		4.55 M	–03.0	1.85 M	–58.5		
		30 M	–103.0	22.4 M	–103.0		
				30 M	–103.0		

NOTE – The PSD profiles are constructed with straight lines between these break frequencies, when plotted against a ***logarithmic*** frequency scale and a ***linear*** dBm scale. The levels are defined with a 135 Ω resistive load.

Table B.8/G.991.2 – Break frequencies of the "XA.R.#" PSD profiles that specify the equivalent disturbance spectra of alien disturbers

XA.R.A [Hz]	135 Ω [dBm/Hz]	XA.R.B [Hz]	135 Ω [dBm/Hz]	XA.R.C [Hz]	135 Ω [dBm/Hz]	XA.R.D [Hz]	135 Ω [dBm/Hz]
1	–20.0	1	–25.7	1	–25.7		
15 k	–20.0	15 k	–25.7	15 k	–25.7		
60 k	–25.2	30 k	–26.8	30 k	–26.8	ALL	–∞
276 k	–25.8	67 k	–31.2	67 k	–31.2		
500 k	–51.9	142 k	–31.2	142 k	–31.2		
570 k	–69.5	156 k	–32.7	156 k	–32.7		
600 k	–69.9	276 k	–33.2	276 k	–33.2		
650 k	–62.4	400 k	–46.0	335 k	–42.0		
763 k	–62.4	500 k	–57.9	450 k	–47.9		
1.0 M	–71.5	570 k	–75.7	750 k	–45.4		
2.75 M	–96.5	600 k	–76.0	1040 k	–45.5		
30 M	–96.5	650 k	–68.3	2.46 M	–63.6		
		763 k	–68.3	23.44 M	–103.0		

Table B.8/G.991.2 – Break frequencies of the "XA.R.#" PSD profiles that specify the equivalent disturbance spectra of alien disturbers

XA.R.A [Hz]	135 Ω [dBm/Hz]		XA.R.B [Hz]	135 Ω [dBm/Hz]		XA.R.C [Hz]	135 Ω [dBm/Hz]		XA.R.D [Hz]	135 Ω [dBm/Hz]
			1.0 M	−77.5		30 M	−103.0			
			2.8 M	−103.0						
			30 M	−103.0						
NOTE – The PSD profiles are constructed with straight lines between these break frequencies, when plotted against a ***logarithmic*** frequency scale and a ***linear*** dBm scale. The levels are defined with a 135 Ω resistive load.										

B.3.5.4.2 Time domain profiles of generators G1-G4

The noise, as specified in the frequency domain in B.3.5.3.1 to B.3.5.3.4, shall be random in nature and near Gaussian distributed. This means that the amplitude distribution function of the combined impairment noise injected at the adding element shall lie between the two boundaries as illustrated in Figure B.6, where the non-shaded area is the allowed region. The boundaries of the mask are specified in Table B.9.

It is expected that noise generators will generate signals that are approximately Gaussian. Therefore, the upper bound of Figure B.6 is lost. PDFs of signals generated by noise generators are expected to be well below the upper bound allowed by the PDF mask shown in Table B.9.

The amplitude distribution function $F(a)$ of noise $u(t)$ is the fraction of the time that the absolute value of $u(t)$ exceeds the value "a". From this definition, it can be concluded that $F(0) = 1$ and that $F(a)$ monotonically decreases up to the point where "a" equals the peak value of the signal. From there on, $F(a)$ vanishes:

$$F(a) = 0 \text{, for } a \geq \left| u_{peak} \right|$$

The boundaries on the amplitude distribution ensure that the noise is characterized by peak values that are occasionally significantly higher than the rms-value of that noise (up to 5 times the rms-value).

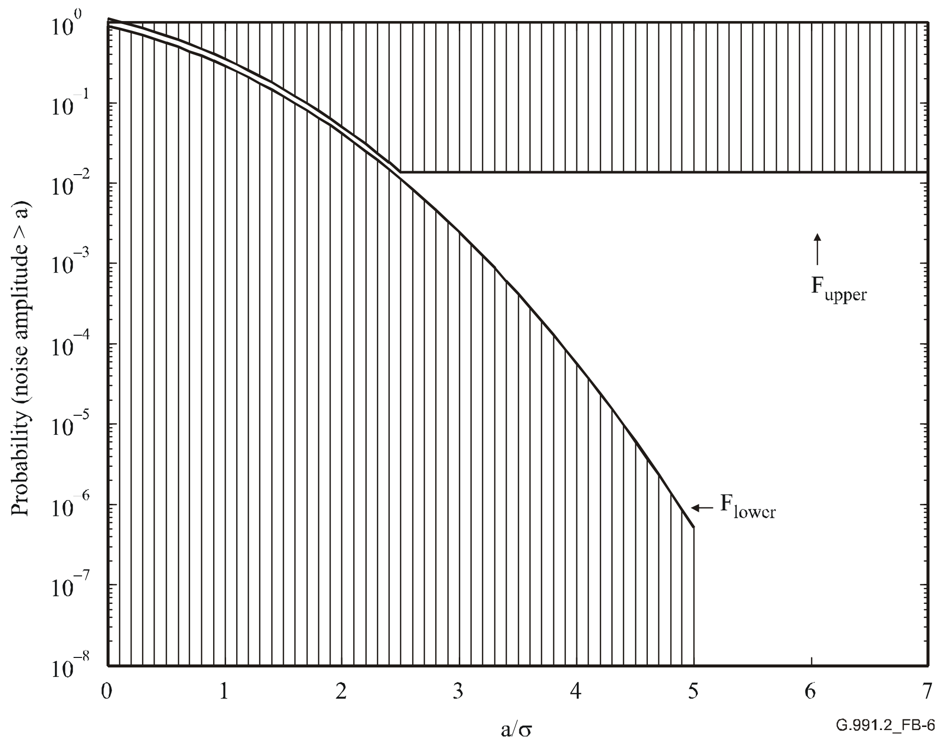


Figure B.6/G.991.2 – Mask for the amplitude distribution function

Table B.9/G.991.2 – Upper and lower boundaries of the amplitude distribution function of the noise

Boundary (σ = rms value of noise)	Interval
$F_{lower}(a) = (1 - \varepsilon) \cdot \{1 - \mathrm{erf}((a/\sigma)/\sqrt{2})\}$	$0 \le a/\sigma < \mathrm{CF}$
$F_{lower}(a) = 0$	$\mathrm{CF} \le a/\sigma < \infty$
$F_{upper}(a) = (1 + \varepsilon) \cdot \{1 - \mathrm{erf}((a/\sigma)/\sqrt{2})\}$	$0 \le a/\sigma < A$
$F_{upper}(a) = (1 + \varepsilon) \cdot \{1 - \mathrm{erf}(A/\sqrt{2})\}$	$A \le a/\sigma < \infty$

Parameter	Value
Crest factor	CF = 5
Gaussian gap	$\varepsilon = 0.1$
	$A = \mathrm{CF}/2 = 2.5$

The meaning of the parameters in Table B.9 is as follows:

– CF denotes the minimum crest factor of the noise, that characterizes the ratio between the absolute peak value and rms value ($\mathrm{CF} = |u_{peak}|/u_{rms}$).

– ε denotes the Gaussian gap that indicates how "close" near Gaussian noise approximates true Gaussian noise.

– *A* denotes the point beyond which the upper limit is alleviated to allow the use of noise signals of practical repetition length.

B.3.5.5 Mandatory noise shape substitution rule

The strict application of the test procedure requires a different noise shape for each test although some of the noise shapes are very similar. In order to reduce the number of possible noise shapes, the following substitution rule is mandatory. It reduces the number of noise shapes from 280 to 22.

Table B.9a tabulates the noise substitution rule. The following nomenclature is used to describe a shape:

"Side (C or R) Rate (384 to 2304) PSDType(s for symmetric) NoiseModel (A to D)"

Example 1: C384sA2 represents the noise shape on the STU-C side for the 384 kbit/s rate using the symmetric PSD corresponding to noise model A and loop 2.

Example 2: C384sAX represents the noise shape on the STU-C side for the 384 kbit/s rate using the symmetric PSD corresponding to noise model A and any loop.

Example 3: Rule 7 requires that the following noise shapes: R384sA1, R384sA2, R384sA3, R384sA4, R384sA5, R384sA6, R384sA7, R512sA1, R512sA2, R512sA3, R512sA4, R512sA5, R512sA6, R512sA7 be replaced by the single noise shape R768sA2.

Example 4: Conducting Test Set 3 of Table B.3 for 384 kbit/s at the STU-C end. The loop and transceiver would be set up as per the test description (Loop #3 upstream set to 43 dB @ 150 kHz, which is equivalent to a length of 5563 m). The transceiver would be set to 384 kbit/s. The noise shape injected would be 'R768sC2' rather than 'C384sD3' (rule 9).

Table B.9a/G.991.2 – Noise shape substitution rule

Rule #	This shape	Replaces those shapes (on a row by row basis)					
1	'C768sA2'	'C384sAX'	'C512sAX'				
2	'C768sC2'	'C384sBX'	'C512sBX'	'C384sCX'	'C512sCX'		
3	'C1536sA2'	'C768sAX'	'C1024sAX'	'C1280sAX'			
4	'C1536sC2'	'C768sBX'	'C1024sBX'	'C1280sBX'	'C768sCX'	'C1024sCX'	'C1280sCX'
5	'C2304sA2'	'C1536sAX'	'C2048sAX'	'C2304sAX'	'C1536sAX'		
6	'C2304sC2'	'C1536sBX'	'C2048sBX'	'C2304sBX'	'C1536sCX'	'C2048sCX'	'C2304sCX'
7	'R768sA2'	'R384sAX'	'R512sAX'				
8	'R768sB2'	'R384sBX'	'R512sBX'				
9	'R768sC2'	'R384sCX'	'R512sCX'	'C384sDX'	'R384sDX'	'C512sDX'	'R512sDX'
10	'R1536sA2'	'R768sAX'	'R1024sAX'	'R1280sAX'	'R1536sAX'		
11	'R1536sB2'	'R768sBX'	'R1024sBX'	'R1280sBX'	'R1536sBX'		
12	'R1536sC2'	'R768sCX'	'R1024sCX'	'R1280sCX'	'R1536sCX'		
13	'R2048sA2'	'R2048sAX'					
14	'R2048sB2'	'R2048sBX'					
15	'R2048sC2'	'R2048sCX'					
16	'R2304sA2'	'R2304sAX'					
17	'R2304sB2'	'R2304sBX'					
18	'R2304sC2'	'R2304sCX'					
19	'C1280sD2'	'C768sDX'	'R768sDX'	'C1280sDX'	'R1280sDX'		
20	'C1536sD2'	'C1024sDX'	'R1024sDX'	'C1536sDX'	'R1536sDX'		
21	'C2048sD2'	'C2048sDX'	'R2048sDX'				
22	'C2304sD2'	'C2304sDX'	'R2304sD'				

B.3.5.6 Measurement of noise margin

At start-up, the level and shape of crosstalk noise or impulse noise are adjusted, while their level is probed at port RX to meet the impairment level specification in B.3.4. This relative level is referred to as 0 dB. The transceiver link is subsequently activated, and the bit error ratio of the link is monitored.

B.3.5.6.1 Measurement of crosstalk noise margin

For measuring the crosstalk margin, the crosstalk noise level of the impairment generator as defined in B.3.5.4.1 shall be increased by adjusting the gain of amplifier A1 in Figure B.5, equally over the full frequency band of the SHDSL system under test, until the bit error ratio is higher than 10^{-7}. This BER will be achieved at an increase of noise of x dB, with a small uncertainty of Δ dB. This value x is defined as the crosstalk noise margin with respect to a standard noise model. The indicated noise margins shall have a tolerance of 1.25 dB due to the aggregate effect of crosstalk generator tolerance and calibrated loop simulator tolerance. The offset Δ is defined using the same procedure as in A.3.1.4.

The noise margins shall be measured (after allowing a minimum 5-minute fine tuning period) using the test loops specified in Figure B.1 and scaled according to Tables B.1 and B.2.

NOTE – Currently, the injected noise, for the purpose of crosstalk noise margin measurement, consists of the sum of generators G1, G2 and G4 as described in B.3.5.1. Appendix IV tabulates the values of the injected noise corresponding to 0 dB margin and a white noise generator value of –140 dBm/Hz. The injected noise should be measured as per B.3.3. The mandatory test cases are described in B.3.4. A mandatory noise substitution rule is described in B.3.5.5.

B.3.5.6.2 Measurement of impulse noise margin

For further study.

B.4 PSD masks

For all data rates, the measured transmit PSD of each STU shall not exceed the PSD masks specified in this clause ($PSDMASK_{SHDSL}(f)$), and the measured total power into 135 Ω shall fall within the range specified in this clause ($P_{SHDSL} \pm 0.5$ dB).

Support for the symmetric PSDs specified in B.4.1 shall be mandatory for all supported data rates. Support for the asymmetric PSDs specified in B.4.2 shall be optional.

Table B.10 lists the supported PSDs and the associated constellation sizes.

Table B.10/G.991.2 – PSD and constellation size

Symmetric PSDs		Asymmetric PSDs			
DS	US	DS	US	DS	US
16-TCPAM	16-TCPAM	16-TCPAM	16-TCPAM	8-TCPAM	16-TCPAM
Mandatory		Optional		For further study	

For the 16-TCPAM upstream and downstream constellations shown in Table B.10, the details of payload data rate, the associated symbol rate, and the mapping of bits per symbol are specified in Table B.11.

Table B.11/G.991.2 – Framed data mode rates

Payload data rate, *R* (kbit/s)	Modulation	Symbol rate (ksymbol/s)	*K* (Bits per symbol)
$R = n \times 64 + (i) \times 8$	16-TCPAM	$(R + 8) \div 3$	3

As specified in clause 5, the allowed rates are given by $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For $n = 36$, i is restricted to the values of 0 or 1.

B.4.1 Symmetric PSD masks

For all values of framed data rate available in the STU, the following set of PSD masks ($PSDMASK_{\text{SHDSL}}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_{sym}} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{Nf_{sym}}\right)\right]^2}{\left(\dfrac{\pi f}{Nf_{sym}}\right)^2} \times \dfrac{1}{1+\left(\dfrac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.5 \text{ MHz} \\ -90\,\text{dBm/Hz peak with maximum power in a } [f, f+1\,\text{MHz}] \text{ window of} & \\ -50\,\text{dBm}, & 1.5\,\text{MHz} < f \le 11.04\,\text{MHz} \end{cases}$$

where $MaskOffsetdB(f)$ is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1 + 0.4 \times \dfrac{f_{3dB} - f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

The inband PSD for $0 < f < 1.5$ MHz shall be measured with a 10 kHz resolution bandwidth.

NOTE 1 – Large PSD variations over narrow frequency intervals (for example near the junction of the main lobe with the noise floor) might require a smaller resolution bandwidth (RBW) to be used. A good rule of thumb is to choose RBW such that there is no more than 1 dB change in the signal PSD across the RBW.

f_{int} is the frequency where the two functions governing $PSDMASK_{SHDSL}(f)$ intersect in the frequency range from 0 to Nf_{sym}. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, N, f_{sym}, f_{3dB}, and P_{SHDSL} are defined in Table B.12. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload data rate.

Table B.12/G.991.2 – Symmetric PSD parameters

Payload data rate, *R* (kbit/s)	K_{SHDSL}	*Order*	*N*	Symbol rate f_{sym} (ksymbol/s)	$f_{3\text{ dB}}$	P_{SHDSL} (dBm)
$R < 2048$	7.86	6	1	$(R + 8)/3$	$1.0 \times f_{\text{sym}}/2$	$P1(R) \le P_{\text{SHDSL}} \le 13.5$
$R \ge 2048$	9.90	6	1	$(R + 8)/3$	$1.0 \times f_{\text{sym}}/2$	14.5

$P1(R)$ is defined as follows:

$$P1(R) = 0.3486 \log_2(R \times 1000 + 8000) + 6.06 \text{ dBm}$$

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure B.7 shows the PSD masks with 0 dB power backoff for payload data rates of 256, 512, 768, 1536, 2048 and 2304 kbit/s.

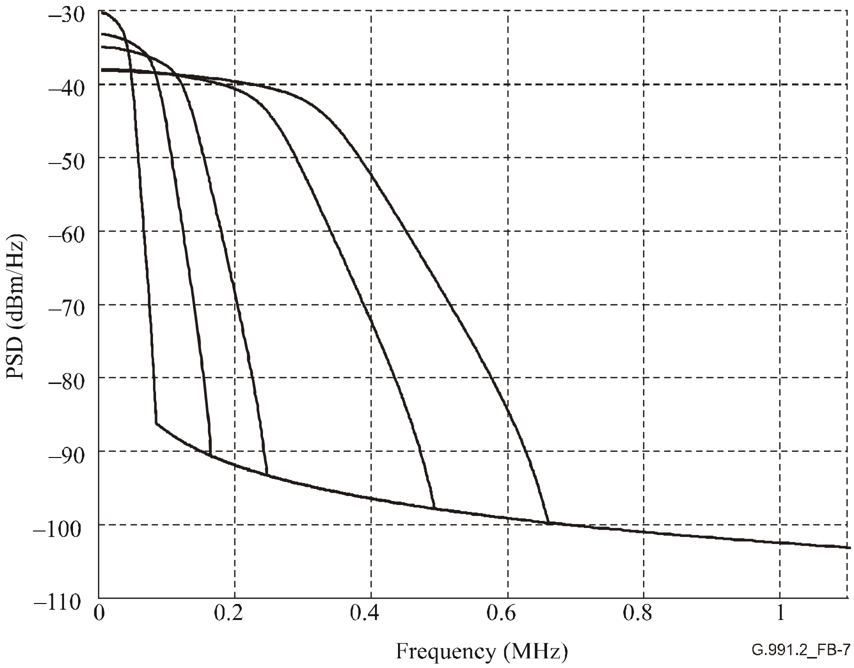


Figure B.7/G.991.2 – PSD masks for 0 dB power backoff

The equation for the nominal PSD measured at the terminals is:

$$Nominal\ PSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_{sym}} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\dfrac{\pi f}{N f_{sym}}\right)^2} \times \dfrac{1}{1+\left(\dfrac{f}{f_{3dB}}\right)^{2\times Order}} \times \dfrac{f^2}{f^2+f_c^2} & , f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5} & , f_{\text{int}} \le f \le 1.5 \text{ MHz} \\ -90 \text{ dBm/Hz peak with maximum power in a } [f,\ f+1 \text{ MHz}] \text{ window of} & \\ -50 \text{ dBm} & , 1.5 \text{MHz} < f \le 11.04 \text{ MHz} \end{cases}$$

where f_c is the transformer cut-off frequency, assumed to be 5 kHz. Figure B.8 shows the nominal transmit PSDs with 13.5 dBm power for payload data rates of 256, 512, 768, 1536, 2048 and 2304 kbit/s.

NOTE 2 – The nominal PSD is given for information only.

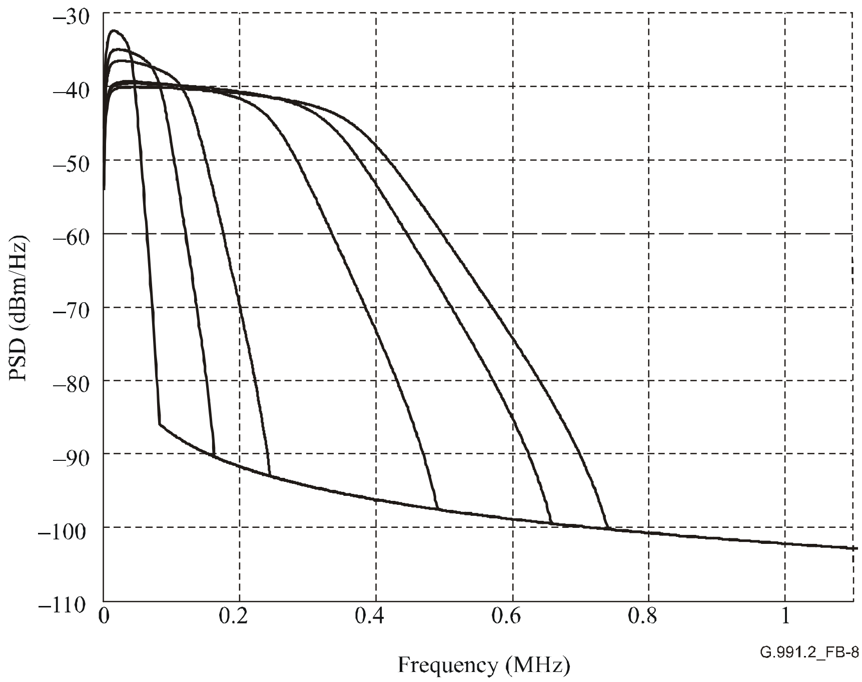


Figure B.8/G.991.2 – Nominal symmetric PSDs for 0 dB power backoff

NOTE 3 – In this clause, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz unless otherwise specified, and *f* is in units of Hz.

B.4.2 Asymmetric 2.048 Mbit/s and 2.304 Mbit/s PSD masks

The asymmetric PSD mask set specified in this clause shall optionally be supported for the 2.048 Mbit/s and the 2.304 Mbit/s payload data rate. Power and power spectral density is measured into a load impedance of 135 Ω.

For the 2.048 Mbit/s and the 2.304 Mbit/s payload data rates available in the STU, the following set of PSD masks ($PSDMASK_{SHDSL}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_x} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{f_x}\right)\right]^2}{\left(\dfrac{\pi f}{f_x}\right)^2} \times \dfrac{1}{1+\left(\dfrac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\text{int}} \\ 0.5683\times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.5 \text{ MHz} \\ -90\,\text{dBm/Hz peak with maximum power in a } [f, f+1 \text{ MHz}] \text{ window of} & \\ -50\,\text{dBm}, & 1.5\,\text{MHz} < f \le 11.04\,\text{MHz} \end{cases}$$

where *MaskOffsetdB*(*f*) is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1 + 0.4 \times \dfrac{f_{3dB} - f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

The inband PSD for $0 < f < 1.5$ MHz shall be measured with a 10 kHz resolution bandwidth.

NOTE 1 – Large PSD variations over narrow frequency intervals (for example near the junction of the main lobe with the noise floor) might require a smaller resolution bandwidth (RBW) to be used. A good rule of thumb is to choose RBW such that there is no more than 1 dB change in the signal PSD across the RBW.

f_{int} is the frequency where the two functions governing $PSDMASK_{SHDSL}(f)$ intersect in the frequency range from 0 to f_x. PBO is the power backoff value in dB. K_{SHDSL}, $Order$, f_x, f_{3dB} and P_{SHDSL} are defined in Table B.13. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. R is the payload data rate.

Table B.13/G.991.2 – Asymmetric PSD parameters

Payload date rate (kbit/s)	Transmitter	K_{SHDSL}	*Order*	f_x (Hz)	f_{3dB} (Hz)	P_{SHDSL} (dBm)
2048	STU-C	16.86	7	1 370 667	548 267	16.25
2048	STU-R	15.66	7	685 333	342 667	16.50
2304	STU-C	12.48	7	1 541 333	578 000	14.75
2304	STU-R	11.74	7	770 667	385 333	15.25

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure B.9 shows the PSD masks with 0 dB power backoff for payload data rates of 2048 and 2304 kbit/s.

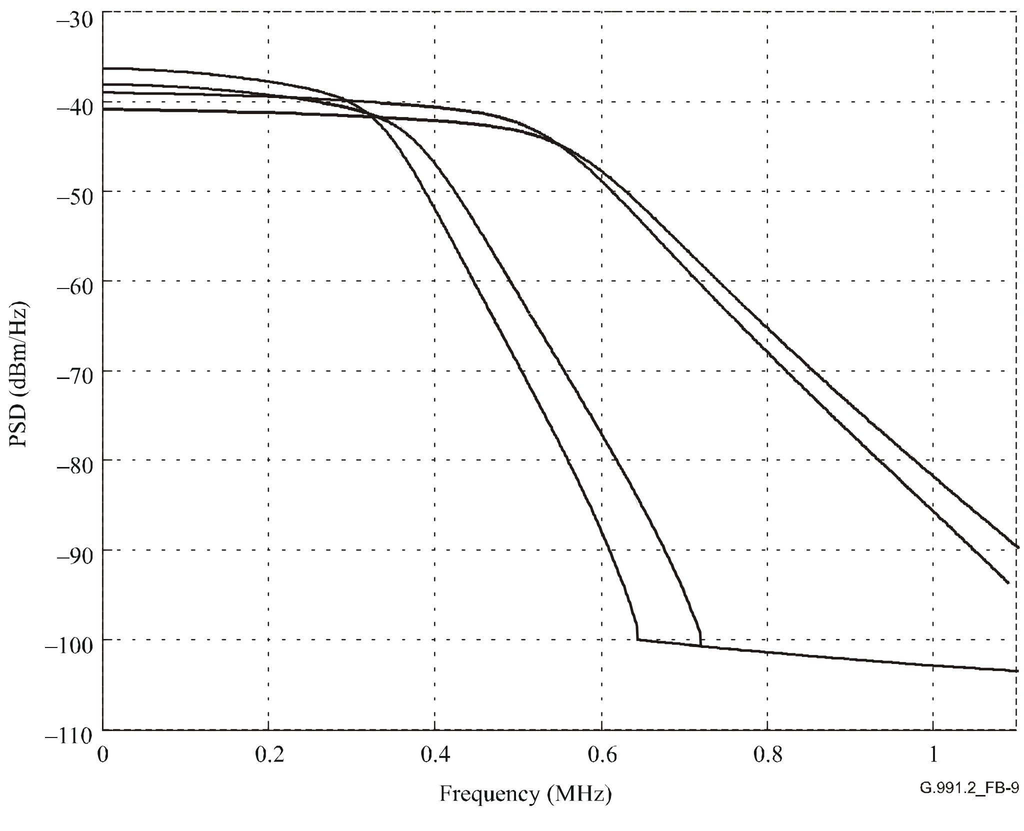


Figure B.9/G.991.2 – PSD masks for 0 dB power backoff

The equation for the nominal PSD measured at the terminals is:

$$NominalPSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_x} \times \frac{\left[\sin\left(\frac{\pi f}{f_x}\right)\right]^2}{\left(\frac{\pi f}{f_x}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times \frac{f^2}{f^2+f_c^2}, f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5}, \qquad f_{\text{int}} \le f \le 1.5 \text{ MHz} \\ -90 \text{ dBm/Hz peak with maximum power in a } [f, f+1\text{MHz}] \text{ window of} \\ -50 \text{ dBm}, \qquad 1.5 \text{ MHz} < f \le 11.04 \text{ MHz} \end{cases}$$

where f_c is the transformer cut off frequency, assumed to be 5 kHz. Figure B.10 shows the nominal transmit PSDs with 0 dB power backoff for payload data rates of 2048 and 2304 kbit/s.

NOTE 2 – The nominal PSD is given for information only.

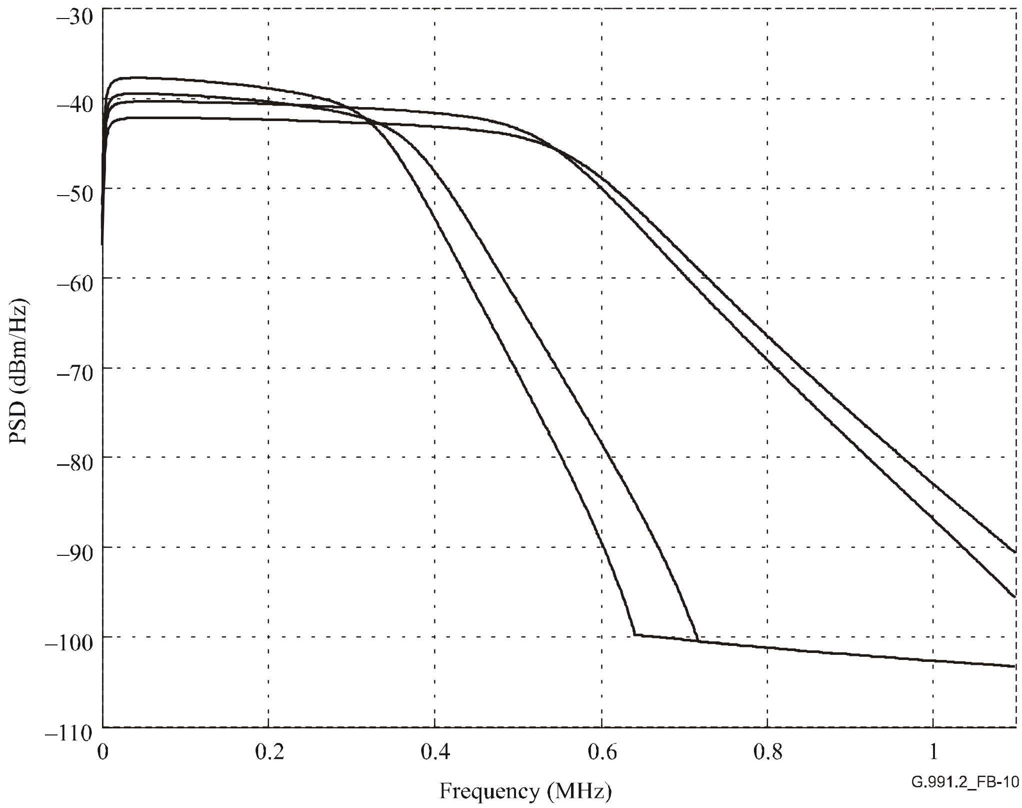


Figure B.10/G.991.2 – Nominal asymmetric PSDs for 0 dB power backoff

NOTE 3 – In this clause, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz unless otherwise specified, and *f* is in units of Hz.

B.5 Region-specific functional characteristics

B.5.1 Data rate

For devices supporting Annex B functionality, no additional limitation on data rates shall be placed beyond the limitations stated in clause 5 and reiterated in 7.1.1, 8.1 and 8.2. For details of the supported symbol rates and their association with PSDs, see B.4.

B.5.2 Return loss

For devices supporting Annex B functionality, return loss shall be specified based on the methodology of 11.3 and the limitations of Figure 11-6. The following definitions shall be applied to the quantities shown in Figure 11-6:

$$RL_{MIN} = 12 \text{ dB}$$

$$f_0 = 12.56 \text{ kHz}$$

$$f_1 = 50 \text{ kHz}$$

$$f_2 = f_{sym}/2$$

$$f_3 = 1.99 f_{sym}$$

where f_{sym} is the symbol rate.

NOTE – The intention of the return loss specification is to maintain some power constraint, even under severe mismatched conditions, when SHDSL modems are connected to real cables. A minimum return loss bounds the (complex) output impedance Z_s within a restricted range around the design impedance $R_v = 135\ \Omega$, and thus the maximum available power from that source. Therefore it is expected that the power dissipated into a complex load impedance Z_L should never exceed the appropriate PSD masks and maximum aggregate powers for all values Z_L in the range of $10\ \Omega < |Z_L| < 2000\ \Omega$, as specified for $R_v = 135\ \Omega$ in B.4 and Tables B.12 and B.13. The extension of the existing power constraints to the severely mismatched case is for further study.

B.5.3 Span powering

B.5.3.1 General

This clause deals with power feeding of the STU-R, regenerators (if required) and the provision of power to the application interface for narrow-band services under restricted conditions (life line circuit). The requirements given in this clause imply compliance to IEC 60950 [7].

B.5.3.2 Power feeding of the STU-R

The STU-R shall be able to consume power from the remote power feeding circuit when the local power supply fails.

NOTE – The remote feeding strategy may not be applicable for extremely long lines or lines including regenerators. In those cases specific feeding methods may be applied, which are for further study.

The STU-R shall be able to draw up to a maximum of 10 mA as wetting current from the remote feeding circuit when the STU-R is being powered locally. When the local power fails, the maximum current drawn by the STU-R from the remote feeding circuit shall be limited to the value specified in IEC 60950 [7].

It is optional for the STU-C to provide wetting current.

B.5.3.3 Power feeding of the interface for narrow-band services

When simultaneous telephone service is provided by the STU-R, feeding of restricted mode power for life line service has to be provided for at least one telephone set in case of local power failure.

NOTE – The remote feeding strategy may not be applicable for extremely long lines or lines including regenerators. In those cases, specific feeding methods may be applied which are for further study.

B.5.3.4 Feeding power from the STU-C

The feeding power shall be limited to the values specified by the TNV requirements in IEC 60950 [7].

NOTE – This means that the sum of the DC- and AC-voltage at the STU-R may not exceed 120 V. The safety standards may for extraordinary cases with long lines or regenerators allow higher power to be supplied from the STU-C. This is left for further study. It is likely that supporting long lines and/or regenerators may imply floating (not connected to ground) power feeding circuits.

B.5.3.5 Power available at the STU-R

The STU-R shall be able to deal with any polarity. With a minimum voltage of 45 V (see Note) at the input of the STU-R, it shall enter a full operational state.

NOTE – This value depends on the supply voltage and is for further study.

When remote power feeding is provided by the network, the STU-R and the side of the SRU directed towards the STU-C shall enter a high impedance state within 2 s after interruption of the remote current fed towards the STU-R or the SRU respectively. This state shall be maintained as long as the voltage on the line stays below 18 V (DC + AC peak). In this state the leakage current shall be less than 10 µA and the capacitance shall be greater than 2 µF. A guard time of at least 2 s between removing the remote power and applying a test voltage is necessary.

B.5.4 Longitudinal balance

For devices supporting Annex B functionality, longitudinal balance shall be specified based on the methodology of 11.1 and the limitations of Figure 11-2. The following definitions shall be applied to the quantities in Figure 11-2.

$$LB_{\mathrm{MIN}} = 40 \text{ dB}$$

$$f_1 = 5 \text{ kHz}$$

$$f_2 = f_{\mathrm{sym}}/2$$

where f_{sym} is the symbol rate.

B.5.5 Longitudinal output voltage

For devices supporting Annex B functionality, longitudinal output voltage shall be specified based on the methodology of 11.2. The measurement frequency range shall be between 100 Hz and 400 kHz.

B.5.6 PMMS target margin

If the optional line probe is selected during the G.994.1 session, the receiver shall use the negotiated target margin. If worst-case PMMS target margin is selected, then the receiver shall assume the disturbers of Table B.14 to determine if a particular rate can be supported. Reference crosstalk shall be computed using the cable crosstalk models of B.3.5.2, assuming infinite loop length so that FEXT components are ignored and NEXT is independent of loop length. The reference crosstalk specified in this clause may not be representative of worst-case conditions in all networks. Differences between crosstalk environments may be compensated by adjusting the target margin.

Table B.14/G.991.2 – Reference disturbers used during PMMS for worst-case target margin

Rate (kbit/s)	PSD (direction)	Reference disturber
All	Symmetric (US/DS)	49 SHDSL
2048	Asymmetric (US)	49 SHDSL-SYM with f_{sym} = 685 333 Hz
2048	Asymmetric (DS)	49 SHDSL-SYM with f_{sym} = 685 333 Hz
2304	Asymmetric (US)	49 SHDSL-SYM with f_{sym} = 770 667 Hz
2304	Asymmetric (DS)	49 SHDSL-SYM with f_{sym} = 770 667 Hz

B.5.7 Span powering in *M*-pair mode

In the optional *M*-pair mode, the requirements for remote power feeding or wetting current for each of the *M* pairs shall be identical to the requirements for a single pair specified in B.5.3.

NOTE – This implies that the powering/wetting current is provided by a potential difference between tip and ring on each of the *M* pairs.

Annex C

Regional requirements – Region 3

See Annex H/G.992.1 [1] for specifications of transceivers for use in networks with existing TCM-ISDN service (as specified in Appendix III/G.961 [B1]).

Annex D

Signal regenerator operation

In order to achieve data transmission over greater distances than are achievable over a single SHDSL segment, one or more signal regenerators (SRUs) may be employed. In the optional *M*-pair mode, *M*-pair regenerators may be used when this reach extension is required. This annex specifies operational characteristics of signal regenerators and the start-up sequence for SHDSL spans containing signal regenerators. Additional explanatory text is included in Appendix III.

D.1 Reference diagram

Figure D.1 is a reference diagram of a SHDSL span containing two regenerators. Up to eight (8) regenerators per span are supported within the EOC addressing scheme (9.5.5.5), and no further limitation is intended herein. Each SRU shall consist of two parts: an SRU-R for interfacing with the STU-C (or a separate SRU-C), and an SRU-C for interfacing with the STU-R (or a separate SRU-R). An internal connection between the SRU-R and SRU-C shall provide the communication between the two parts during start-up and normal operation. An SHDSL span containing *X* regenerators shall contain $X + 1$ separated SHDSL segments, designated TR1 (STU-C to SRU_1), TR2 (SRU_X-C to STU-R), and RR*n* (SRU_n-C to SRU_{n+1} – R, where $1 \le n \le X - 1$). Each segment shall follow the general principles described in 6.2, 6.3 and 7.2 for the pre-activation and activation procedures. Additional requirements specific to spans containing regenerators are described in this annex.

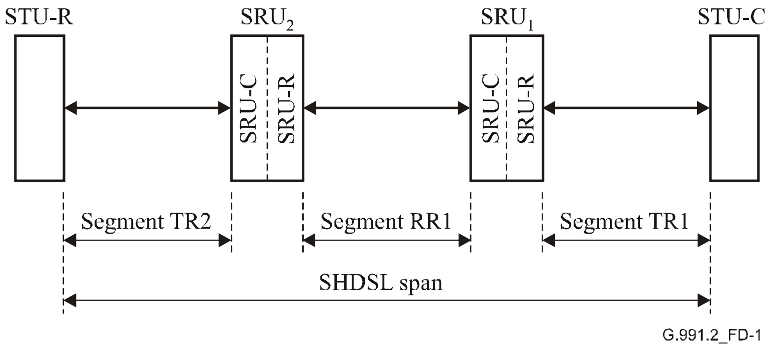


Figure D.1/G.991.2 – Block diagram of a SHDSL span with two signal regenerators

D.2 Start-up procedures

D.2.1 SRU-C

Figure D.2 shows the State Transition Diagram for SRU-C start-up and operation. The SRU-C begins in the "Idle" state and, in the case of an STU-R initiated start-up, transitions first to the "Wait for STU-C" state. For an STU-C initiated start-up, the SRU-C moves from "Idle" to the "G.994.1 Session 1" state. An SRU initiated start-up shall function identically to an STU-C initiated start-up from the perspective of the SRU-C.

The SRU-C shall communicate "Capabilities Available" status and transfer a list of its capabilities to the SRU-R across the regenerator's internal interface upon entering the "Wait for STU-C" state. The SRU-C's capabilities list, as transferred to the SRU-R, shall be the intersection of its own capabilities, the capabilities list it received from the STU-R (or SRU-R) in its G.994.1 session, and the segment capabilities determined by the line probe, if used.

The SRU-C shall receive mode selection information from the SRU-R in association with the "SRU-R Active" indication. In the subsequent G.994.1 session, the SRU-C shall select the same mode and parameter settings for the SHDSL session.

The timer T_{SRUC} shall be set to 4 minutes. If T_{SRUC} expires before the SRU-C reaches the "Active" state, the SRU-C shall return to the "Idle" state and shall indicate link failure to the SRU-R across the internal interface. The SRU-C shall also indicate failure and return to the "Idle" state if a G.994.1 initiation is unsuccessful after 30 s.

The "Diagnostic Mode" bit, if set in the G.994.1 Capabilities Exchange, shall cause an SRU-C to function as an STU-C if the subsequent segment fails. This implies that an internal failure indication received while in the "Wait for STU-C" state shall cause the SRU-C to select an operational mode, initiate a G.994.1 session, and transition to state "G.994.1 Session 2".

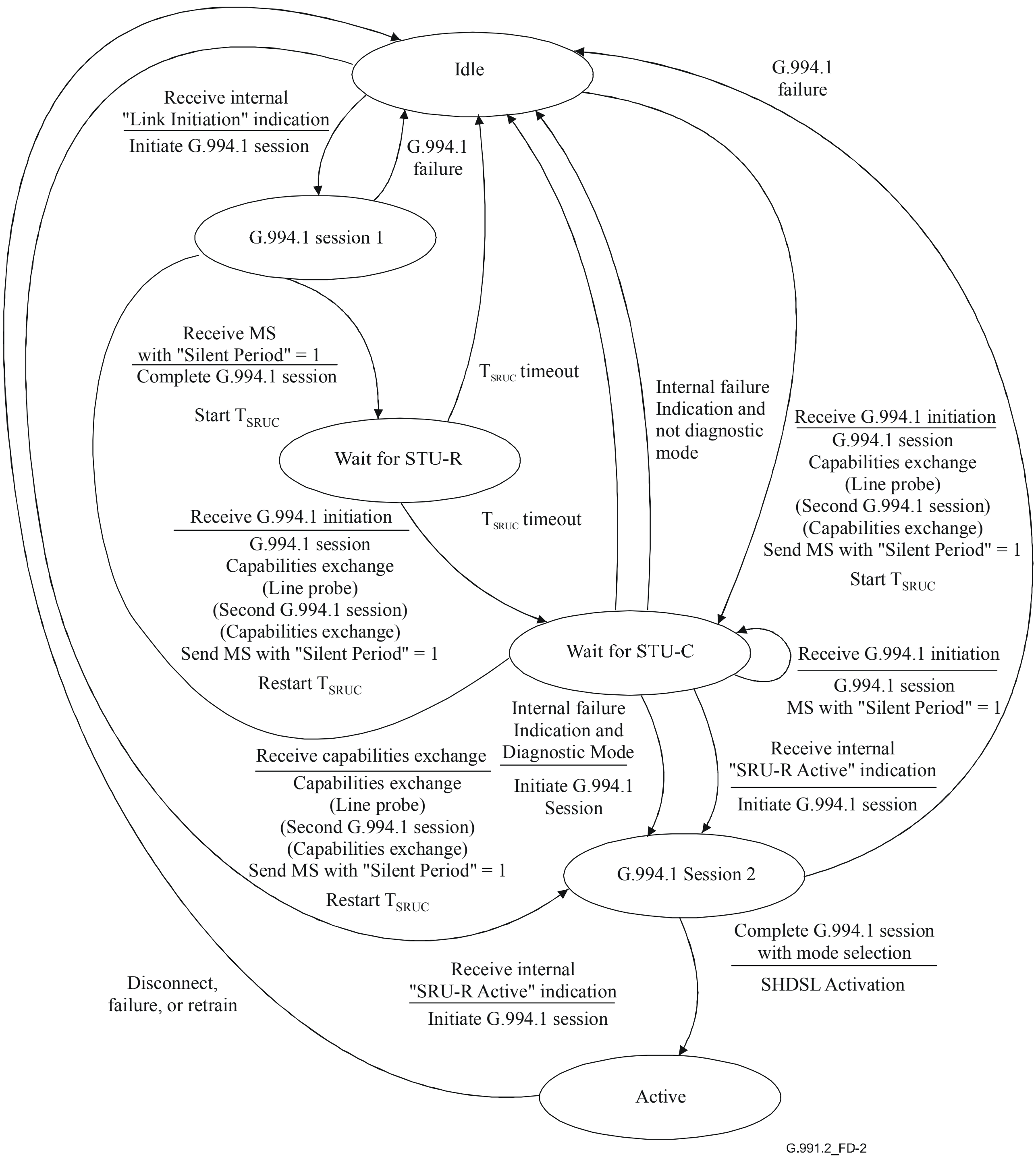


Figure D.2/G.991.2 – SRU-C state transition diagram

D.2.2 SRU-R

Figure D.3 shows the State Transition Diagram for SRU-R start-up and operation. The SRU-R begins in the "Idle" state and, in the case of an STU-R initiated train, transitions first to the "G.994.1 Session 1" state. For an STU-C initiated train, the SRU-C moves from "Idle" to the "G.994.1 Session 2" state.

The SRU-R shall communicate "Link Initiation" status to the SRU-C across the regenerator's internal interface upon entering the "Wait for STU-R" state. Upon entering the "Active" state, it shall communicate "SRU-R Active" status to the SRU-C. If plesiochronous operation (Clock Mode 1; see clause 10) is selected, the SRU-R may optionally indicate its entry into the "Active" state to the SRU-C prior to the completion of the SHDSL activation sequence. If synchronous or network referenced plesiochronous clocking is selected (Clock Modes 2, 3a or 3b; see clause 10), the SRU-R shall not indicate entry into the "Active" state until the SHDSL activation sequence has been completed.

The SRU-R shall receive a list of capabilities from the SRU-C across the regenerator's internal interface in association with the "Capabilities Available" indication. The SRU-R's capabilities list, as indicated in the subsequent G.994.1 session, shall be the intersection of its own capabilities with the capabilities list it received from the SRU-C.

The SRU-R shall provide mode selection information to the SRU-C in association with the "SRU-R Active" indication, based on the selections it has received in the G.994.1 session.

The timer T_{SRUR} shall be set to 4 minutes. If T_{SRUR} expires before the SRU-R reaches the "Active" state, the SRU-R shall return to the "Idle" state and shall indicate link failure to the SRU-C across the internal interface. The SRU-R shall also indicate failure and return to the "Idle" state if a G.994.1 initiation is unsuccessful after 30 s.

The "Diagnostic Mode" bit, if set in the G.994.1 Capabilities Exchange, shall cause an SRU-R to function as an STU-R if the subsequent segment fails. This implies that an internal failure indication received while in the "Wait for STU-R" state shall cause the SRU-R to initiate a G.994.1 session and transition to state "G.994.1 Session 2".

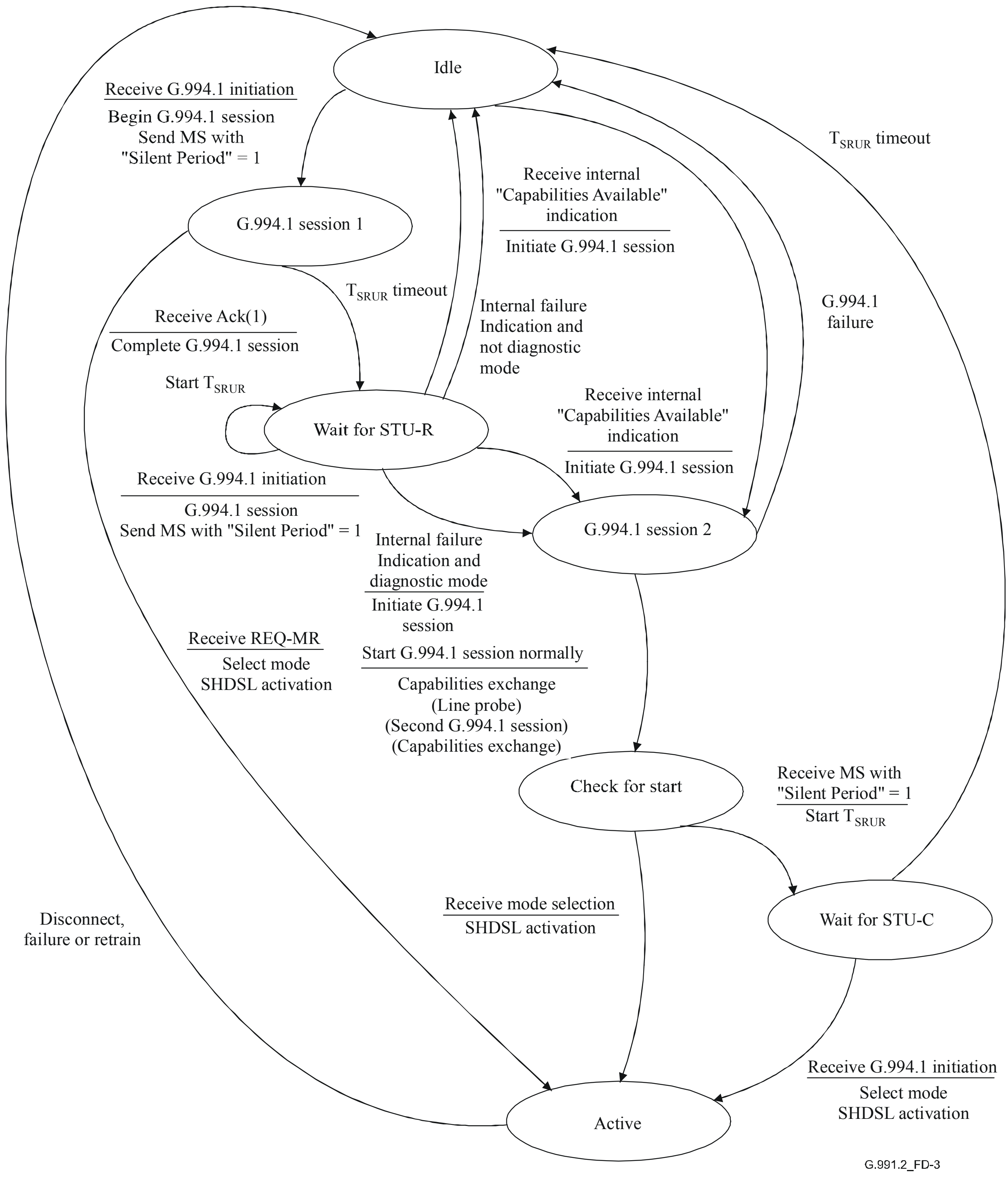


Figure D.3/G.991.2 – SRU-R state transition diagram

D.2.3 STU-C

In order to support operation with regenerators, each STU-C shall support the Regenerator Silent Period (RSP) bit, as specified in ITU-T Rec. G.994.1. Second, the STU-C shall not indicate a training failure or error until it has been forced into "silent" mode for at least 5 consecutive minutes.

D.2.4 STU-R

In order to support operation with regenerators, each STU-R shall support the Regenerator Silent Period (RSP) bit, as specified in ITU-T Rec. G.994.1. The STU-R shall not indicate a training failure or error until it has been forced into "silent" mode for at least 5 consecutive minutes.

D.2.5 Segment failures and retrains

In the case of a segment failure or a retrain, each segment of the span shall be deactivated, with each SRU-C and each SRU-R returning to its "Idle" state. The restart may then be initiated by the SRU, the STU-R, or the STU-C.

D.3 Symbol rates

For Annex A operational modes, signal regenerators may transmit at symbol rates up to and including 280 ksymbol/s in either two-wire or the optional *M*-pair mode. This corresponds, for 16-TCPAM, to maximum user data rates (not including framing overhead) of 832 kbit/s and $M \times 832$ kbit/s for two-wire and *M*-pair operation, respectively. Operation at higher symbol rates is for further study.

For Annex B operational modes, signal regenerators may transmit at symbol rates up to and including 685.33 ksymbol/s in either two-wire or the optional *M*-pair mode. This corresponds, for 16-TCPAM, to maximum user data rates (not including framing overhead) of 2.048 Mbit/s and $M \times 2.048$ Mbit/s for two-wire and *M*-pair operation, respectively. Operation at higher symbol rates is for further study.

In either case, each STU and SRU on a span shall select the same operational data rate.

D.4 PSD masks

Any of the PSDs from Annex A or Annex B may be used for the TR1 segment (STU-C to SRU_1-R), as appropriate to the given region. All other segments shall employ one of the appropriate symmetric PSDs, as described in either A.4.1 or B.4.1. The selection of PSD shall be limited by the symbol rate considerations of D.3.

Annex E

Application-specific TPS-TC framing

This annex provides implementation details for the various types of TPS-TC framing that may be supported by SHDSL transceivers. The TPS-TC framing mode is selected during pre-activation, but the criteria for selecting a particular TPS-TC mode are application-specific and are beyond the scope of this Recommendation.

E.1 TPS-TC for clear channel data

In Clear Channel mode, there shall be no specified relationship between the structure of the user data and its positioning within the Payload Sub-Blocks. k_s bits of contiguous user data shall be contained within each Sub-Block, as specified in 8.1. The temporal relationship between the user data stream and the data within the Sub-Blocks shall be maintained such that the order of bits in time from the user data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. Any additional structure within the user data shall be maintained by an unspecified higher layer protocol and is outside the scope of this Recommendation.

In the optional M-pair mode, clear channel data will be carried over all pairs using interleaving, as described in 8.2. The bitstream of the user data consisting of $M \times k_s$ bits is mapped to the M pairs by placing alternating bitstreams consisting of k_s bits of contiguous user data in each of the M SHDSL channels. k_s bits of contiguous user data shall be contained within a Sub-Block on Pair 1, and the following sets of k_s bits of contiguous user data shall be contained within the corresponding Sub-Blocks of subsequent pairs. As noted above, any additional structure within the user data shall be maintained by an unspecified higher layer protocol and is outside the scope of this Recommendation.

E.2 TPS-TC for clear channel byte-oriented data

In the byte-oriented clear channel mode, the input byte stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing n 8-bit time slots. Each byte from the input data stream is mapped LSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot n. A total of k_s bits (or n bytes) of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Note that optional extensions described in Annex F allow values of n up to 89. See Figure E.1 for additional details.

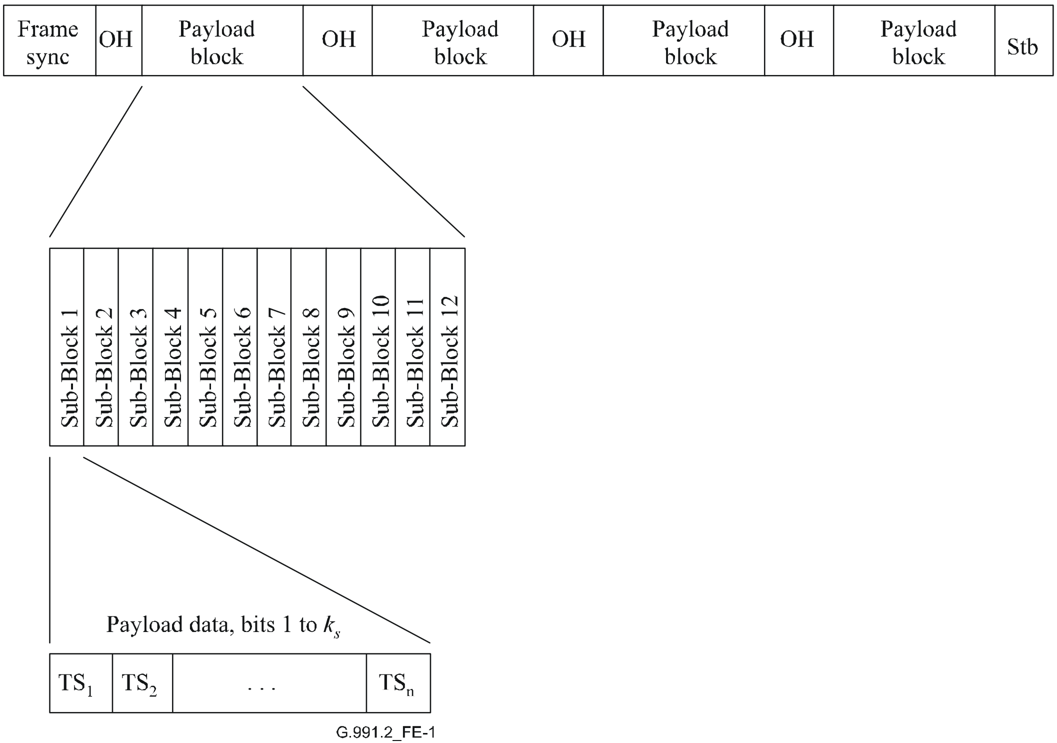


Figure E.1/G.991.2 – Clear channel byte-oriented framing

In the optional M-pair mode, byte-oriented data is carried over all M pairs using interleaving, as described in 8.2. A total of $M \times k_s$ bits ($M \times n$ bytes) of byte-oriented data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Note that optional extensions described in Annex F allow values of n up to 89. Only numbers of time slots divisible by M may be supported in M-pair mode. The input byte stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing $M \times n$ 8-bit time slots. Each byte from the input data stream is mapped LSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot n. A total of $M \times k_s$ bits (or

$M \times n$ bytes) of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_S = i + n \times 8$, and, in this mode, $i = 0$ and $3 \leq n \leq 36$. The bytes from the input data stream shall be interleaved among all M pairs, such that pair M carries the mth byte out of every block of M bytes. See Figure E.2 for additional details.

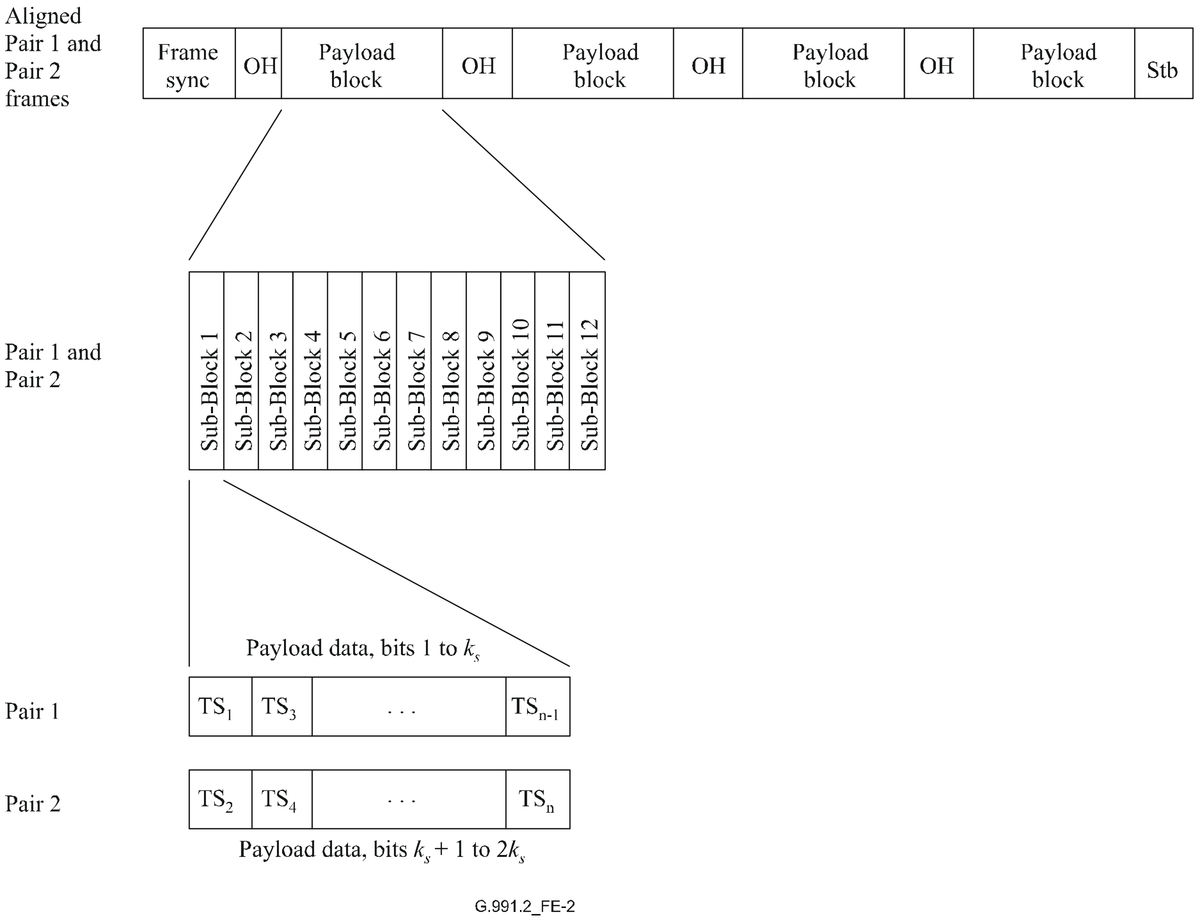


Figure E.2/G.991.2 – *M*-pair framing for byte-oriented clear channel (for the *M* = 2 case)

E.3 TPS-TC for unaligned DS1 transport

Much of the data within the North American network is structured as "DS1" data streams, which, for purposes of this Recommendation, can be described as 1.544 Mbit/s data streams containing 8 kHz framing, with each frame containing 24 8-bit time slots and one framing bit. Details of DS1 framing and associated data structure can be found in 2.1/G.704 [B6].

In Unaligned DS1 mode, there shall be no specified relationship between the DS1 frames and their positioning within the Payload Sub-Blocks. A total of k_S bits of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_S = i + n \times 8$, and, in this mode, $n = 24$ and $i = 1$. The DS1 framing clocks shall be synchronized to the SHDSL clocks such that the DS1 frame always appears in the same position within each SHDSL Payload Sub-Block; however, no particular alignment is specified. The temporal relationship between the DS1 data stream and the data within the Sub-Blocks shall be maintained, such that the order of bits in time from the DS1 data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. The optional *M*-pair mode will not support Unaligned DS1 transport.

E.4 TPS-TC for aligned DS1/fractional DS1 transport

As noted in E.3, "DS1" data streams consist of 1.544 Mbit/s data streams containing 8 kHz framing, with each frame containing 24 8-bit time slots and one framing bit. In some cases, "Fractional DS1" data streams are used, where DS1 frames contain less than the normal 24 8-bit time slots. Aligned DS1/Fractional DS1 mode is also applicable to 1.544 Mbit/s PRI (Primary Rate ISDN), as described in 4.2/I.431 [B10].

In Aligned DS1/Fractional DS1 mode, each DS1 frame shall be aligned within the SHDSL Payload Sub-Block such that the DS1 framing bit occupies the first bit position within the Payload Sub-Block, followed by time slot 1, time slot 2, … , time slot n. A total of k_S bits of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_S = i + n \times 8$, and, in this mode, $i = 1$. In DS1 applications, $n = 24$, and, in Fractional DS1 applications, $3 \le n < 24$. The DS1 framing clocks shall be synchronized to the SHDSL clocks such that the DS1 frame always appears in the defined position within each SHDSL Payload Sub-Block. See Figure E.3 for additional details.

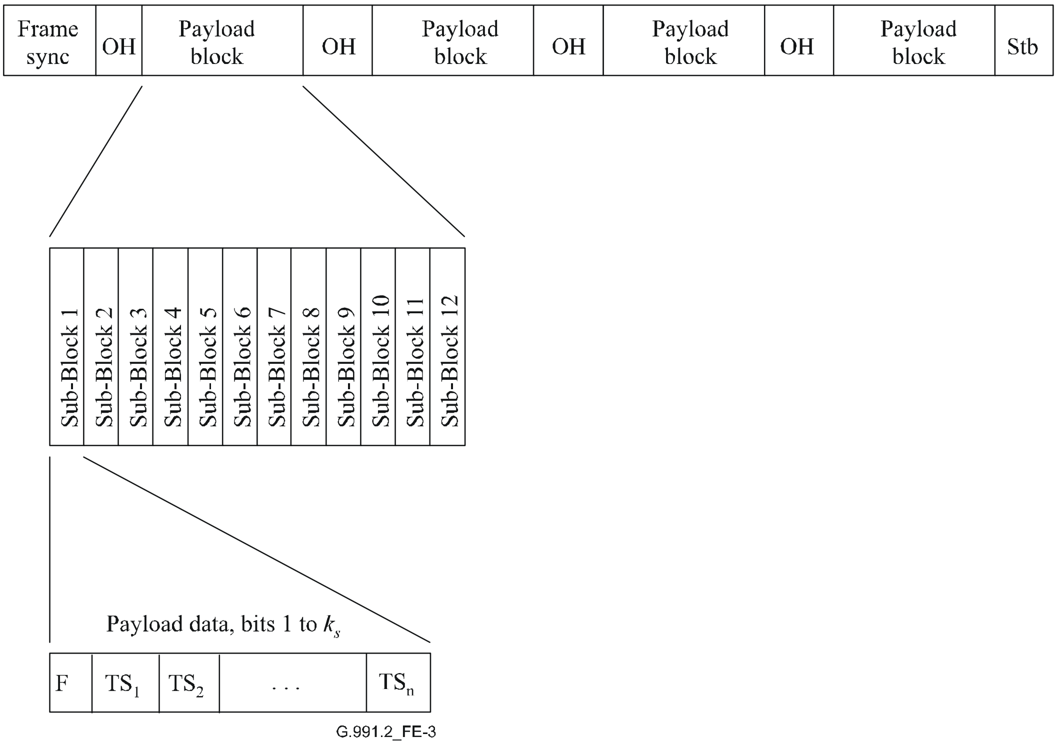


Figure E.3/G.991.2 – Aligned DS1/fractional DS1 framing

In the optional M-pair mode, DS1/Fractional DS1 data will be carried over all M pairs using interleaving, as described in 8.2. A total of $M \times (k_S - 1) + 1$ bits of DS1/Fractional DS1 data shall be transported per SHDSL Payload Sub-Block. $k_S = i + n \times 8$, and, in this mode, $i = 1$. In DS1 applications, $n = 24/M$, and in Fractional DS1 applications, $3 \le n < 24/M$. In M-pair mode only multiples of M DS1 time slots may be supported. Each DS1 frame shall be aligned within the SHDSL Payload Sub-Block such that the DS1 framing bit occupies the first bit position within the Payload Sub-Block on each of the M wire pairs. The time slots of the DS1 frame shall be interleaved among all M wire pairs, such that pair M carries the mth time slot out of every block of M slots. See Figure E.4 for additional details.

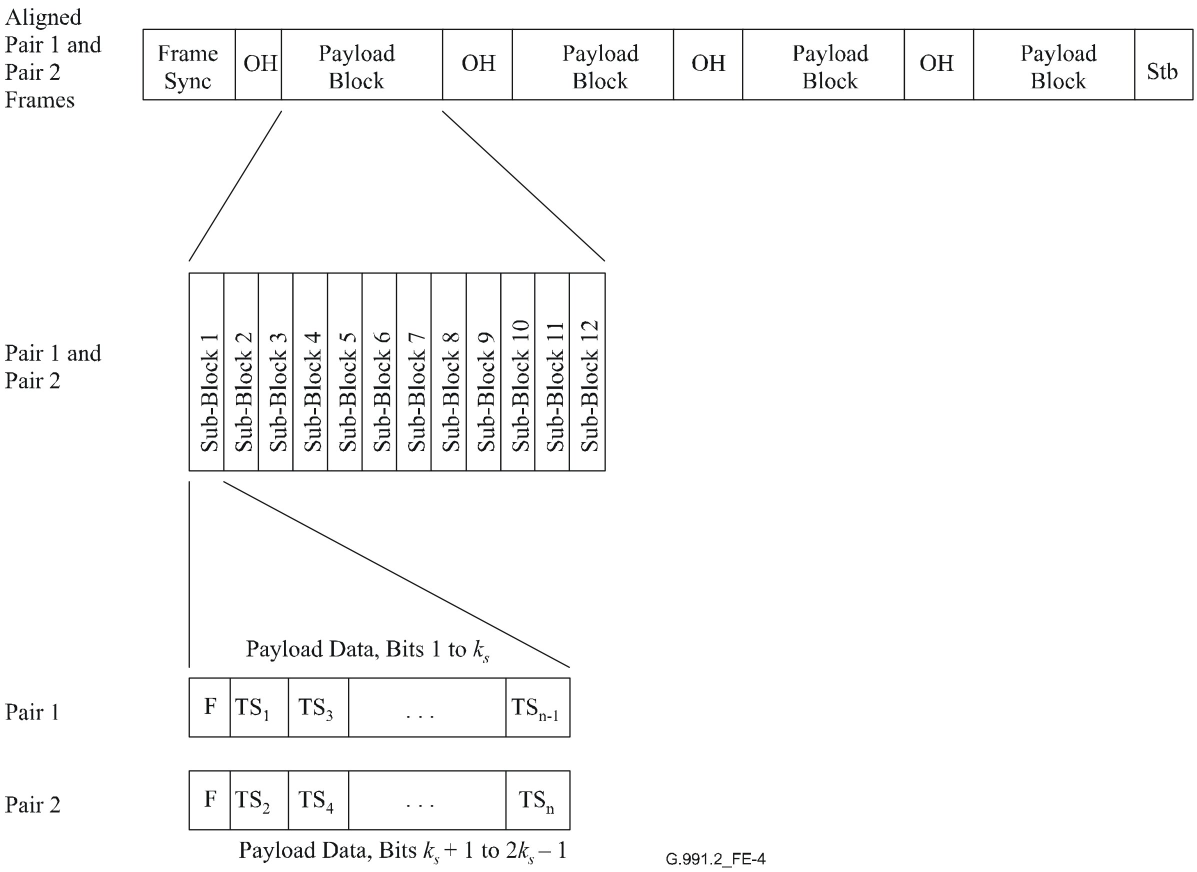


Figure E.4/G.991.2 – *M*-Pair framing for DS1/fractional DS1 (for the *M* = 2 case)

E.5 TPS-TC for European 2048 kbit/s digital unstructured leased line (D2048U)

D2048U data streams contain unstructured 2.048 Mbit/s data with no specified framing. These data streams shall be carried using the Clear Channel TPS-TC described in E.1.

E.6 TPS-TC for unaligned European 2048 kbit/s digital structured leased line (D2048S)

Much of the data within the European network is structured as D2048S data streams, which, for purposes of this Recommendation, can be described as 2.048 Mbit/s data streams containing 8 kHz framing, with each frame containing 32 8-bit time slots. Details of D2048S framing and associated data structure can be found in 2.3/G.704 [B6].

In Unaligned D2048S mode, there shall be no specified relationship between the D2048S frames and their positioning within the Payload Sub-Blocks. A total of k_S bits of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_S = i + n \times 8$, and, in this mode, $n = 32$ and $i = 0$. The D2048S framing clocks shall be synchronized to the SHDSL clocks such that the D2048S frame always appears in the same position within each SHDSL Payload Sub-Block; however, no particular alignment is specified. The temporal relationship between the D2048S data stream and the data within the Sub-Blocks shall be maintained, such that that the order of bits in time from the D2048S data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. The optional *M*-pair mode will not support Unaligned D2048S transport.

E.7 TPS-TC for aligned European 2048 kbit/s digital structured leased line (D2048S) and fractional

As noted in E.6, D2048S data streams consist of 2048 Mbit/s data streams containing 8 kHz framing, with each frame containing 32 8-bit time slots. In some cases, Fractional D2048S data streams are used, where frames contain less than the normal 32 8-bit time slots. Aligned D2048S mode is also applicable to 2.048 Mbit/s PRI (Primary Rate ISDN), as described in 5.2/I.431 [B10].

In the aligned D2048S mode, each D2048S frame shall be aligned within the SHDSL Payload Sub-Block such that the first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot *n*. A total of k_s bits of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_s = i + n \times 8$, and, in this mode, $i = 0$. In D2048S applications, $n = 32$, and, in Fractional D2048S applications, $3 \le n < 32$. The D2048S framing clocks shall be synchronized to the SHDSL clocks such that the D2048S frame always appears in the defined position within each SHDSL Payload Sub-Block. See Figure E.5 for additional details.

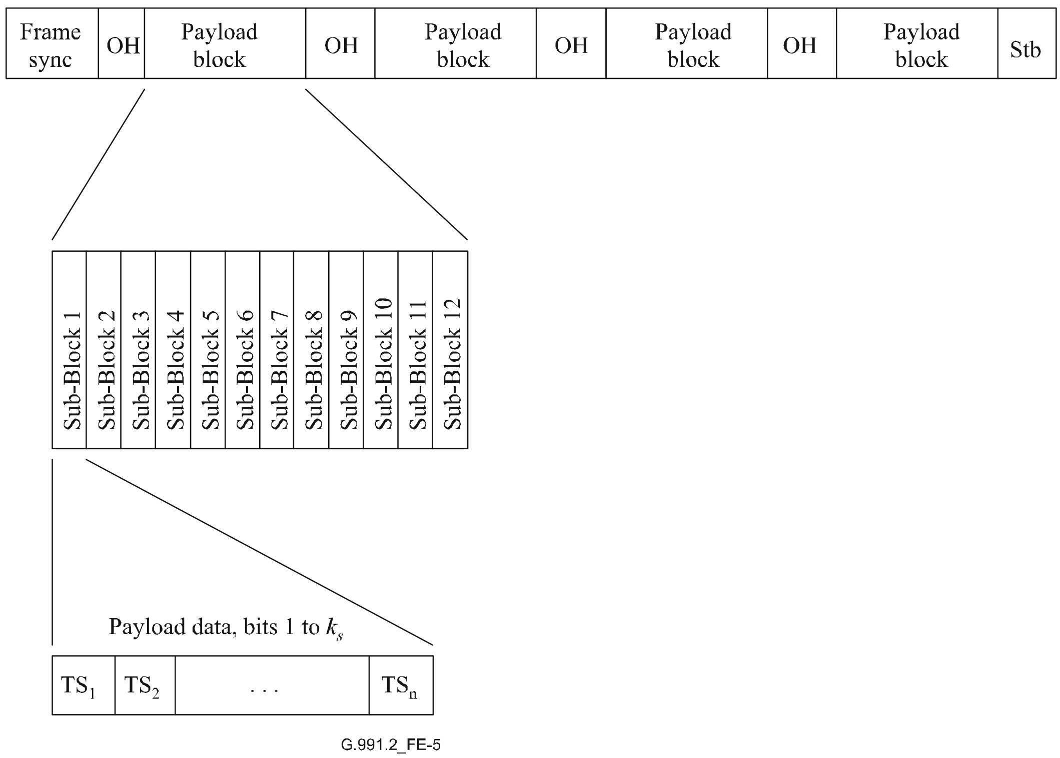


Figure E.5/G.991.2 – Aligned D2048S/fractional D2048S framing

In the optional *M*-pair mode, D2048S/Fractional D2048S data will be carried over all *M* pairs using interleaving, as described in 8.2. A total of $M \times k_s$ bits of D2048S/Fractional D2048S data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n \times 8$, and, in this mode, $i = 0$. In D2048S applications, $n = 32/M$, and in Fractional DS1 applications, $3 \le n < 32/M$. In *M*-pair mode, only multiples of *M* D2048S time slots may be supported. The time slots of the D2048S frame shall be interleaved among all *M* wire pairs, such that pair *M* carries the *m*th time slot out of every block of *M* slots. See Figure E.6 for additional details.

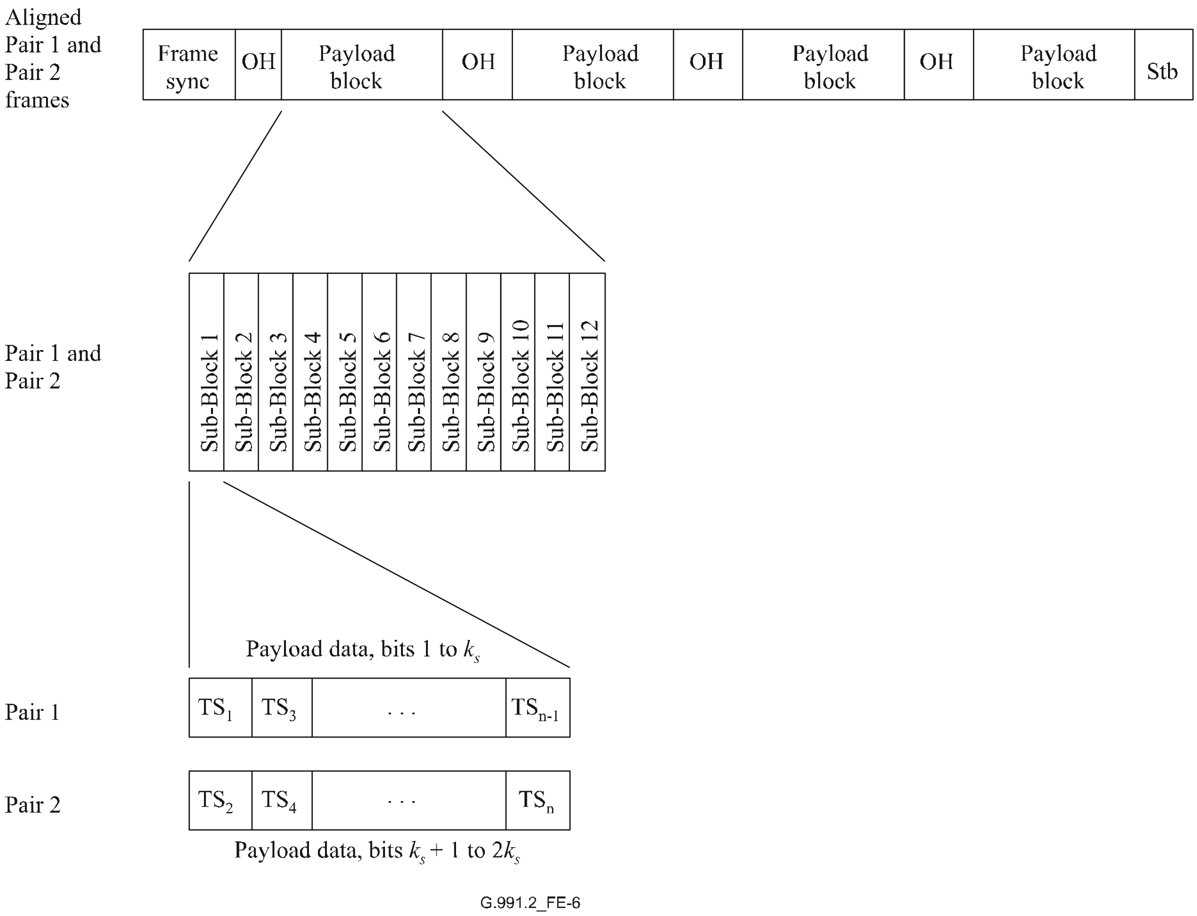


Figure E.6/G.991.2 – *M*-Pair framing for aligned D2048S/fractional D2048S (for the *M* = 2 case)

E.8 TPS-TC for synchronous ISDN basic access

In this TPS-TC mode, the mapping of the ISDN customer data channels to SHDSL payload channels is specified for synchronous transport of multiple ISDN BAs (Basic Access) using clock mode 3a (see 10.1).

The ISDN customer data channels are embedded into the payload data within the SHDSL frames. ISDN channels and SHDSL frames (and any other TPS-TC if Dual-Bearer mode is utilized – see E.10) are synchronized to the same clock domain.

E.8.1 ISDN BA over SHDSL frames

Figure E.7 illustrates typical transport of ISDN BAs within the SHDSL frames. The basic characteristics of this transport are as follows:

- B-channels and D-channels are mapped on SHDSL payload channels.
- The ISDN BA does not need a separate synchronization since the SHDSL frames are synchronized to the same clock domain. Therefore, the ISDN frame word (12 kbit/s) is not needed.
- The ISDN M-channel transports ISDN line status bits, transmission control information as well as signalling to control the ISDN connection. Only the ISDN M-channel functions which are needed to control the interface to the ISDN terminal equipment are transported over a messaging channel (SHDSL EOC or fast signalling channel).

E.8.2 Mapping of ISDN B- and D-channels on SHDSL payload channels

The ISDN B- and D- channels are transported within the SHDSL payload sub-blocks. The SHDSL payload data is structured within the SHDSL frames as follows:

- Each payload sub-block contains $k_s = i + n \times 8$ bits ($i = 0..7$ and $n = 3..36$, or, optionally, $n = 37…89$, as described in Annex F).
- Each sub-block is ordered in the following way: i 1-bit time slots followed by n 8-bit time slots.
- 1-bit time slots are referred to as Z-bits, and 8-bit time slots are referred to as TS_1 ... TS_n.

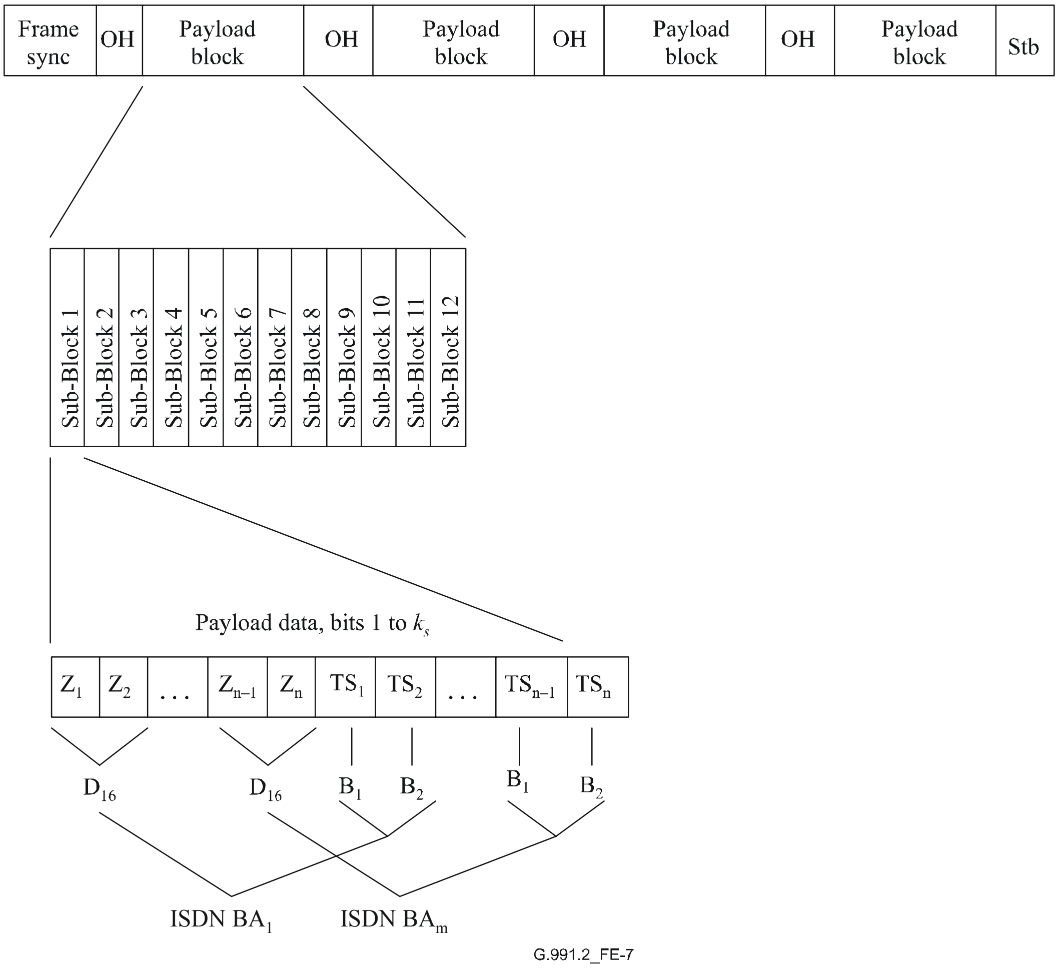


Figure E.7/G.991.2 – Mapping of ISDN B- and D-channels

The payload sub-blocks are composed of combinations of $n \times 8$ bit-TS time slots and $i \times 1$-bit Z-time slots:

- n corresponds to the number of 64 kbit/s payload channels;
- i corresponds to the number of 8 kbit/s channels

This payload structure allows efficient mapping of ISDN BA channels on SHDSL frames.

- Data channels (64 kbit/s each, designated $B_1 – B_y$) are mapped onto 64 kbit/s TS-channels.
- Signalling channels (16 kbit/s each, designated $D_1 – D_x$) are mapped onto two 8 kbit/s Z-channels each.[3]

[3] If four or more ISDN BAs are transported, four D_{16} channels are mapped on one 64 kbit/s B-channel.

A general example of this mapping technique is shown in Figure E.7.

E.8.3 Multi-ISDN BAs

The transport of up to six ISDN BAs is described in detail in the next paragraphs. Figure E.8 shows a mapping example for two ISDN BAs.

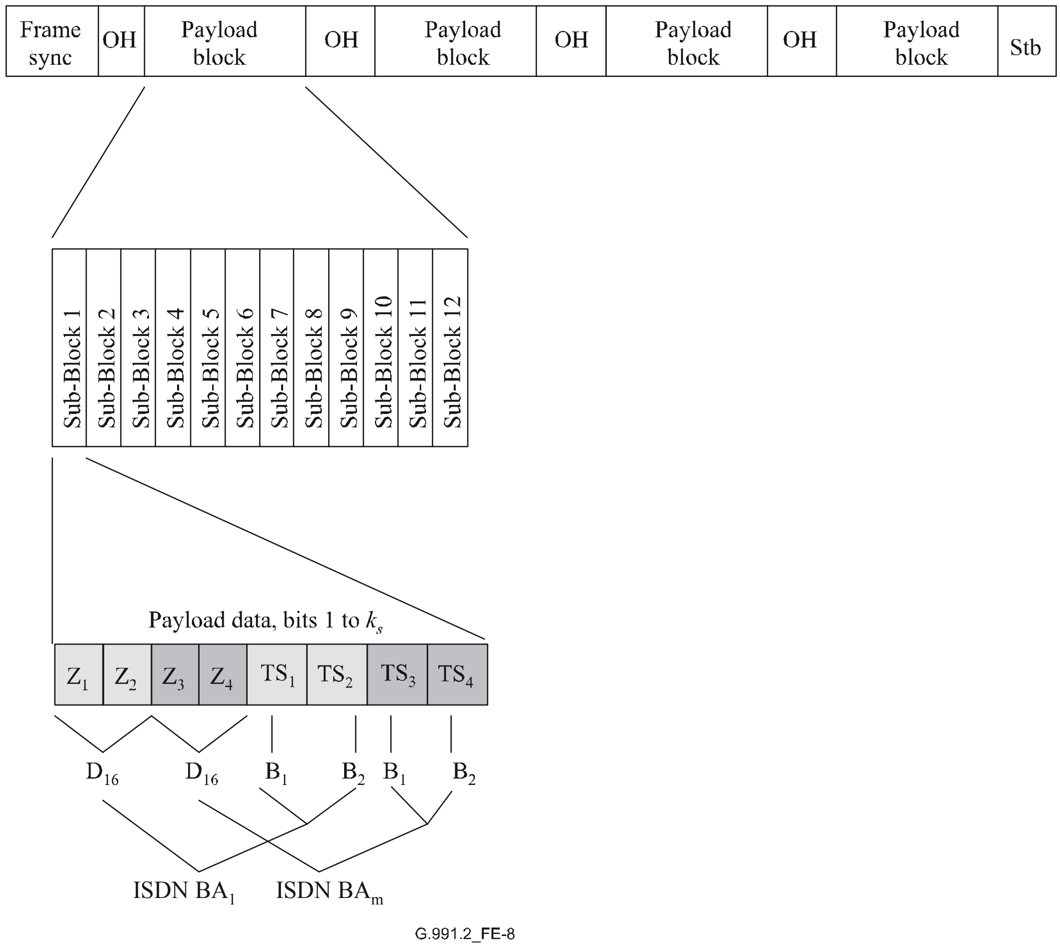


Figure E.8/G.991.2 – Framing example: 2 × ISDN BA

The transport of the customer data channels of each ISDN BA requires 144 kbit/s bandwidth. Table E.1 shows the number of required TS- and Z-channels.

Table E.1/G.991.2 – K × ISDN BA

Number of ISDN BA ***K***	Payload bit rate K × (128 kbit/s + 16 kbit/s)	Application	TS-channels (64 kbit/s) ***n***	Z-channels (8 kbit/s) ***i***
1	144	1 ISDN BA	2	2
2	288	2 ISDN BA	4	4
3	432	3 ISDN BA	6	6
4	576	4 ISDN BA	9	0
5	720	5 ISDN BA	11	2
6	864	6 ISDN BA	13	4

E.8.4 ISDN BA for lifeline service

Lifeline service in case of local power failure can be provided by one ISDN BA. The lifeline BA always is that one which is transported over the first time slots of each payload sub-block (e.g., Z_1, Z_2, TS_1, TS_2). Remote power feeding is provided by the central office such that the transceiver can operate in a reduced power mode.

E.8.5 Time slot positions of ISDN B- and D_{16}-channels (EOC signalling)

If multiple ISDN BAs are transported over SHDSL, certain data channels in the SHDSL payload blocks must be assigned to each ISDN BA. Tables E.2 to E.5 show the allocation of the ISDN data channels of up to 4 BAs. The signalling is transmitted over the SHDSL EOC.

In order to avoid unnecessary shifting of ISDN D- and B-bits, the respective D-bits are transmitted after their B-bits in the subsequent SHDSL payload sub-block (B-bits in *Nth* payload sub-block and D-bits in $N + 1$th payload sub-block; if the B-bits are transmitted in the last payload sub-block of an SHDSL frame, the D-bits are transmitted in the first payload sub-block of the next SHDSL frame).

Table E.2/G.991.2 – Time slot allocation for 1 ISDN BA

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_1 + Z_2$

Table E.3/G.991.2 – Time slot allocation for 2 ISDN BAs

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_1 + Z_2$
2	TS_3	TS_4	$Z_3 + Z_4$

Table E.4/G.991.2 – Time slot allocation for 3 ISDN BAs

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_1 + Z_2$
2	TS_3	TS_4	$Z_3 + Z_4$
3	TS_5	TS_6	$Z_5 + Z_6$

Table E.5/G.991.2 – Time slot allocation for 4 ISDN BAs

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_2	TS_3	TS_1 (Bits 1 and 2)
2	TS_4	TS_5	TS_1 (Bits 3 and 4)
3	TS_6	TS_7	TS_1 (Bits 5 and 6)
4	TS_8	TS_9	TS_1 (Bits 7 and 8)

E.8.5.1 Time slot positions of ISDN B- and D_{16}-channels (EOC signalling) in *M*-pair mode

In the optional *M*-pair mode, the allocation of up to 3 ISDN BAs to time slots and Z-bits shall be as shown in Tables E.2 to E.4. The allocation for 4 ISDN BAs is shown in Table E.5a.

Table E.5a/G.991.2 – Time slot allocation for 4 ISDN BAs

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_1 + Z_2$
2	TS_3	TS_4	$Z_3 + Z_4$
3	TS_5	TS_6	$Z_5 + Z_6$
4	TS_7	TS_8	$Z_7 + Z_8$

The Z-bits and time slots shall be interleaved among all *M* wire pairs. See Figure E.8a for additional details.

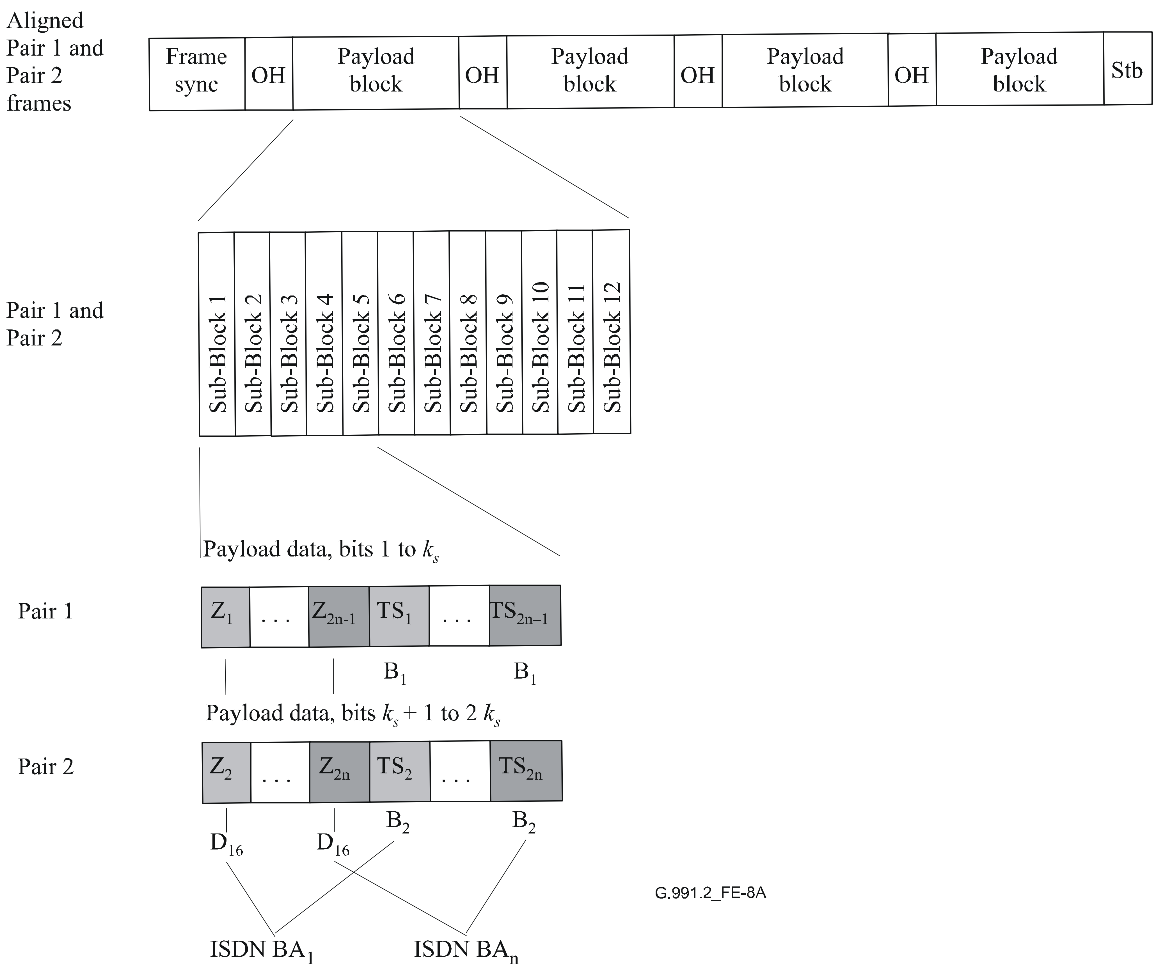


Figure E.8a/G.991.2 – *M*-pair framing for ISDN BA (for the *M* = 2 case)

E.8.6 Time slot positions of ISDN B- and D_{16}-channels and the optional fast signalling channel

The optional 8 kbit/s fast signalling channel is always conveyed in Z_1, as shown in Figure E.9. If this fast signalling channel is used, up to 6 ISDN BAs can be transported over SHDSL.

In order to avoid unnecessary shifting of ISDN D- and B-bits, the respective D-bits are transmitted after their B-bits in the subsequent SHDSL payload sub-block (B-bits in *Nth* payload sub-block and D-bits in *N + 1th* payload sub-block; if the B-bits are transmitted in the last payload sub-block of an SHDSL frame, the D-bits are transmitted in the first payload sub-block of the next SHDSL frame).

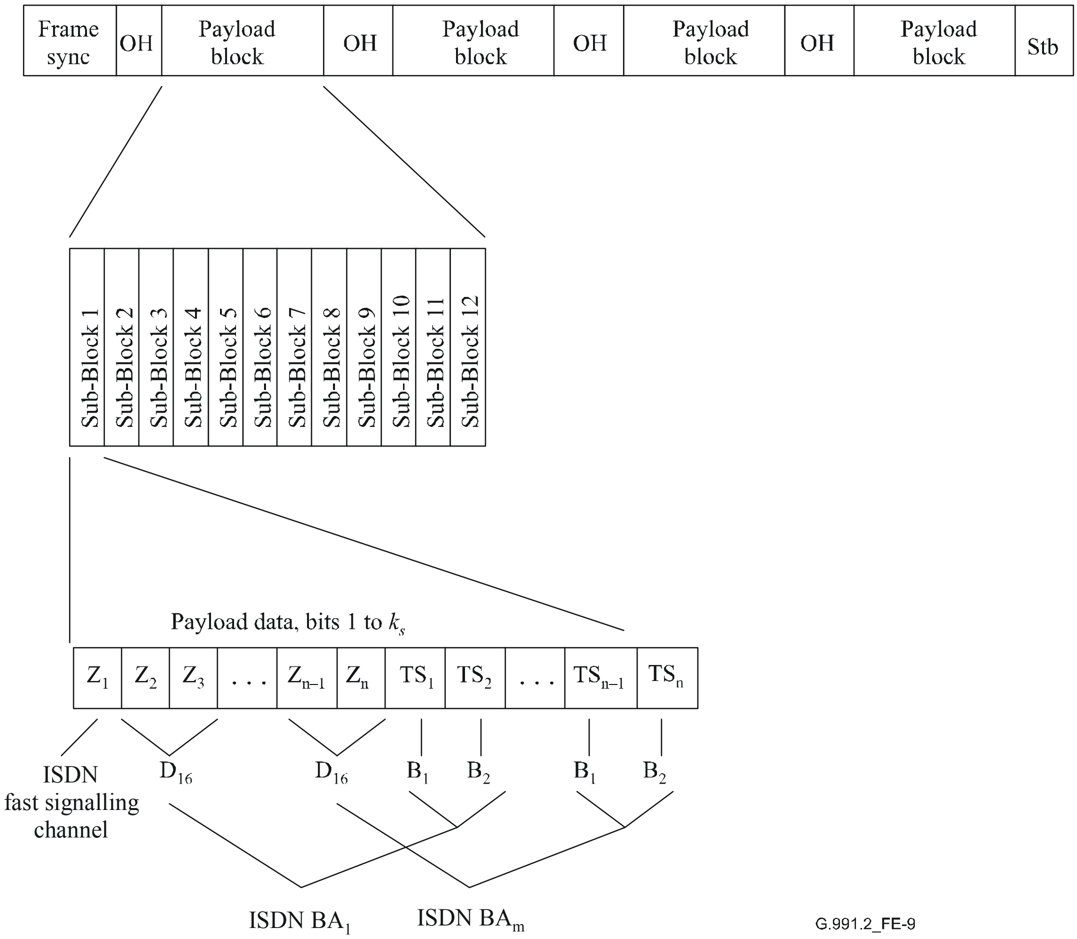


Figure E.9/G.991.2 – Mapping of ISDN B- and D-channels with a fast signalling channel

Table E.6/G.991.2 – Time slot allocation for 1 ISDN BA using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$

Table E.7/G.991.2 – Time slot allocation for 2 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$
2	TS_3	TS_4	$Z_4 + Z_5$

Table E.8/G.991.2 – Time slot allocation for 3 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$
2	TS_3	TS_4	$Z_4 + Z_5$
3	TS_5	TS_6	$Z_6 + Z_7$

Table E.9/G.991.2 – Time slot allocation for 4 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_2	TS_3	TS_1 (Bits 1 and 2)
2	TS_4	TS_5	TS_1 (Bits 3 and 4)
3	TS_6	TS_7	TS_1 (Bits 5 and 6)
4	TS_8	TS_9	TS_1 (Bits 7 and 8)

Table E.10/G.991.2 – Time slot allocation for 5 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_2	TS_3	$Z_2 + Z_3$
2	TS_4	TS_5	TS_1 (Bits 1 and 2)
3	TS_6	TS_7	TS_1 (Bits 3 and 4)
4	TS_8	TS_9	TS_1 (Bits 5 and 6)
5	TS_{10}	TS_{11}	TS_1 (Bits 7 and 8)

Table E.11/G.991.2 – Time slot allocation for 6 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_2	TS_3	$Z_2 + Z_3$
2	TS_4	TS_5	$Z_4 + Z_5$
3	TS_6	TS_7	TS_1 (Bits 1 and 2)
4	TS_8	TS_9	TS_1 (Bits 3 and 4)
5	TS_{10}	TS_{11}	TS_1 (Bits 5 and 6)
6	TS_{12}	TS_{13}	TS_1 (Bits 7 and 8)

E.8.6.1 Time slot positions of ISDN B- and D_{16}-channels (fast signalling) in *M*-pair mode

In the optional *M*-pair mode, the allocation of up to 3 ISDN BAs to Time Slots and Z-bits shall be as shown in Tables E.6 to E.8. The allocation for 4 to 6 ISDN BAs is shown in Tables E.11a to Table E.11c.

Table E.11a/G.991.2 – Time slot allocation for 4 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$
2	TS_3	TS_4	$Z_4 + Z_5$
3	TS_5	TS_6	$Z_6 + Z_7$
4	TS_7	TS_8	$Z_8 + Z_9$

Table E.11b/G.991.2 – Time slot allocation for 5 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$
2	TS_3	TS_4	$Z_4 + Z_5$
3	TS_5	TS_6	$Z_6 + Z_7$
4	TS_7	TS_8	$Z_8 + Z_9$
5	TS_9	TS_{10}	$Z_{10} + Z_{11}$

Table E.11c/G.991.2 – Time slot allocation for 6 ISDN BAs using the fast signalling channel

ISDN BA number	ISDN B_1 time slot	ISDN B_2 time slot	ISDN D_{16} time slots
1	TS_1	TS_2	$Z_2 + Z_3$
2	TS_3	TS_4	$Z_4 + Z_5$
3	TS_5	TS_6	$Z_6 + Z_7$
4	TS_7	TS_8	$Z_8 + Z_9$
5	TS_9	TS_{10}	$Z_{10} + Z_{11}$
6	TS_{11}	TS_{12}	$Z_{12} + Z_{13}$

In fast signalling mode, the time slots and Z-bits frame shall be aligned within the SHDSL Payload Sub-Block such that the Z_1 fast signalling bit occupies the first bit position within the Payload Sub-Block on each of the *M* pairs. The remaining Z-bits and time slots shall be interleaved alternating among all *M* pairs. See Figure E.9a for additional details.

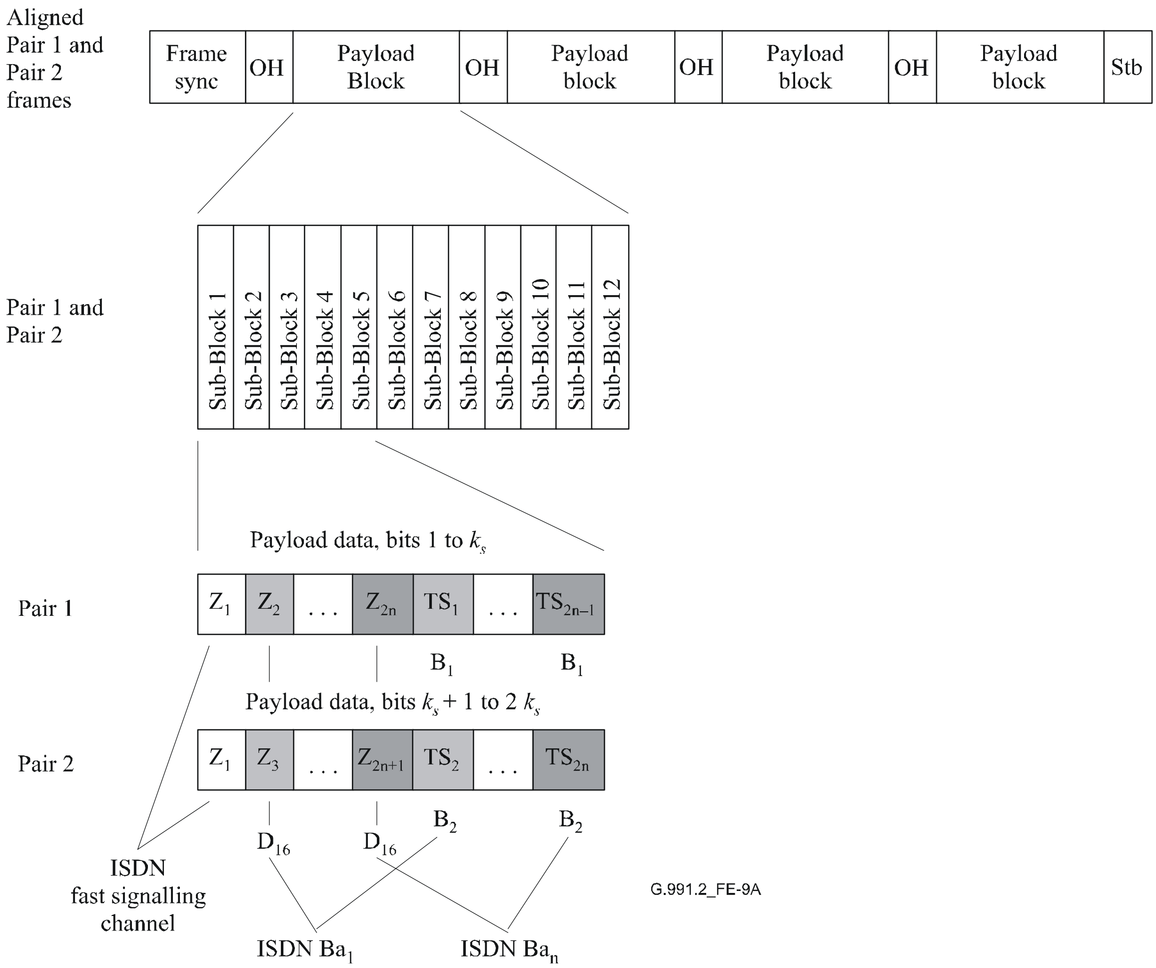


Figure E.9a/G.991.2 – *M*-pair framing for ISDN BA (for the *M* = 2 case)

E.8.7 Signalling over the SHDSL EOC or the fast signalling channel

The ISDN status signalling information can be optionally transmitted over two different channels:

- SHDSL EOC.
- Fast signalling channel.

In both cases, SHDSL EOC messages with their HDLC-like format are used to transport the ISDN message code. The STU-C as well as the STU-R unit can initiate EOC messages. Generally, the ISDN related EOC messages are transported over the SHDSL EOC. In some applications, it is necessary to set up an additional fast signalling channel with 8 kbit/s bandwidth for these ISDN related EOC messages. This is the case when more than four ISDN BAs are used. It may also be used when low latency signalling is required or when another TPS-TC's signalling (e.g., ATM) has substantially restricted the use of the SHDSL EOC channel.

E.8.7.1 SHDSL EOC messages

The EOC messages number 20 and 148 are used to transmit the ISDN maintenance and control functions as well as the other ISDN EOC messages.

Table E.12/G.991.2 – ISDN Request – Message ID 20

Octet #	Contents	Data type	Reference
1	Message ID 20	Message ID	
2 bits 4-7	ISDN BA Number	Unsigned char	
2 bits 0-3	Unused		Set to 0000_2
3	ISDN message code		

Table E.13/G.991.2 – ISDN Response – Message ID 148

Octet #	Contents	Data type	Reference
1	Message ID 148	Message ID	
2 bits 4-7	ISDN BA Number	Unsigned char	
2 bits 0-3	Unused		Set to 0000_2
3	ISDN message code		

ISDN BA Number: Each ISDN BA can be addressed independently. To each ISDN BA, a four-digit number is assigned (BA 1 = 0000, ... BA 6 = 0101).

E.8.7.2 ISDN message codes

The message codes which are contained as an octet in the SHDSL EOC message "ISDN Requests" are listed in Table E.14. The message codes which are contained as an octet in the SHDSL EOC message "ISDN Response" are listed in Table E.15.

Table E.14/G.991.2 – ISDN message codes commands

Function	Message	EOC message code	Comment
S-Bus Control	SIA	0001 0000	S-interface activate (STU-C → STU-R)
	SID	0001 0001	S-interface deactivate (STU-C → STU-R)
	SAI	0001 0010	S-interface activated (STU-R → STU-C)
	SDI	0001 0011	S-interface deactivated (STU-R → STU-C)
ISDN Transceiver Status	ACT	0000 0001	Readiness for layer 2 communication (STU-C → STU-R) (STU-R → STU-C)
	DEA	0000 0010	Intention to deactivate (STU-C → STU-R)
	CSO	0000 0011	Cold start only (STU-R → STU-C)
BA Termination Reset	S reset	0000 0000	Reset of ISDN control unit at STU-R (STU-C → STU-R)

Table E.14/G.991.2 – ISDN message codes commands

Function	Message	EOC message code	Comment
ISDN EOC Messages	Operate 2B + D loopback	0011 0001	(STU-C → STU-R)
	Operate B1-channel loopback (Note)	0011 0010	(STU-C → STU-R)
	Operate B2-channel loopback (Note)	0011 0011	(STU-C → STU-R)
	Return to normal	0011 1111	(STU-C → STU-R)
	Hold state	0011 0000	(STU-C → STU-R)
NOTE – The use of B1- and B2-channel loopbacks is optional. However, the loopback codes are reserved for these functions.			

Table E.15/G.991.2 – ISDN Message codes responses

Function	Message	EOC message code	Comment
S-Bus Control	SIA	1001 0000	S-interface activated
	SIAF	1101 0000	S-interface activation failed
	SID	1001 0001	S-interface deactivated
	SIDF	1101 0001	S-interface deactivation failed
	SAI	1001 0010	S-interface activated
	SDI	1001 0011	S-interface deactivated
ISDN Transceiver Status	ACT	1000 0001	Readiness for layer 2 communication
	DEA	1000 0010	Intention to deactivate
	CSO	1000 0011	Cold start only
BA Termination Reset	S reset ack	1000 0000	Reset of ISDN control unit at STU-R

Table E.15/G.991.2 – ISDN Message codes responses

Function	Message	EOC message code	Comment
ISDN EOC Messages	Operate 2B + D loopback (success)	1011 0001	S-interface activate with loop2
	Operate 2B + D loopback (failure)	1111 0001	
	Operate B1-channel loopback (success)	1011 0010	Operate B1-channel loop can be requested whenever the SHDSL link is activated
	Operate B1-channel loopback (failure)	1111 0010	
	Operate B2-channel loopback (success)	1011 0011	Operate B2-channel loop can be requested whenever the SHDSL link is activated
	Operate B2-channel loopback (failure)	1111 0011	
	Return to normal (success)	1011 1111	
	Return to normal (failure)	1111 1111	
	Hold state	1011 0000	
	Unable to comply acknowledgement	1111 0100	

E.8.8 S-bus control

The ISDN S-buses which connect the ISDN terminals with the STU-R can be controlled independently with the respective message codes (SIA, SID, SAI, SDI) for each S-bus. The STU-C side can activate and deactivate the S bus and gets status information. These messages are transmitted as SHDSL EOC messages.

The S-interfaces of each ISDN BA can be addressed independently. To each ISDN BA a four-digit number is (BA 1 = 0000, ... BA 6 = 0101) contained in the ISDN related SHDSL EOC messages.

SIA: In STU-C to STU-R direction, this function is used to request the STU-R to activate the interface at the S reference point. If the interface at the S reference point is to be activated, this message may be sent. In STU-R to STU-C direction the respective response is SIA (S-Interface Activated).

SID: In STU-C to STU-R direction, this function is used to request the STU-R to deactivate the interface at the S reference point. If the interface at the S reference point is to be deactivated, this message may be sent. In STU-R to STU-C direction the respective response is SID (S-Interface Deactivated).

SAI: In STU-R to STU-C direction, this message is used to inform the STU-C that the S-interface and S-bus have been activated.

SDI: In STU-R to STU-C direction, this message is used to inform the STU-C that the S-interface and S-bus have been deactivated.

E.8.9 BA termination reset

The status and condition of each ISDN BA and its S-interface at the STU-R side can be individually monitored from the STU-C side. If a failure or blocking at one ISDN BA is detected, this situation can be resolved by a reset. "BA termination reset" puts the control unit of the S-interface to its default state (the deactivated state). Other BAs or other services are not affected.

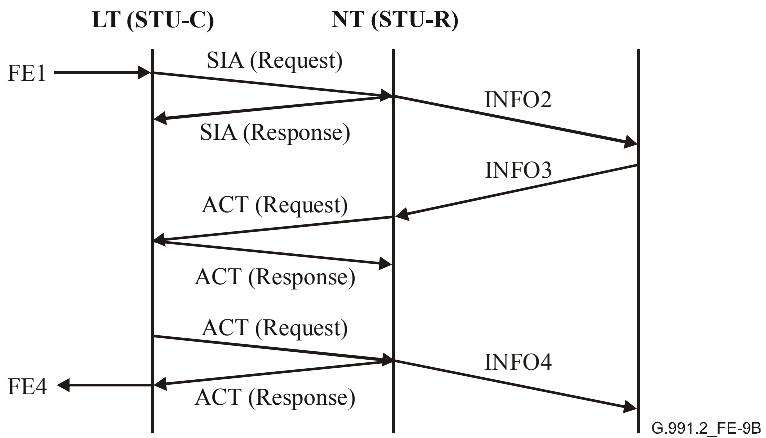


Figure E.9b/G.991.2 – ISDN BA activation initiated by the exchange

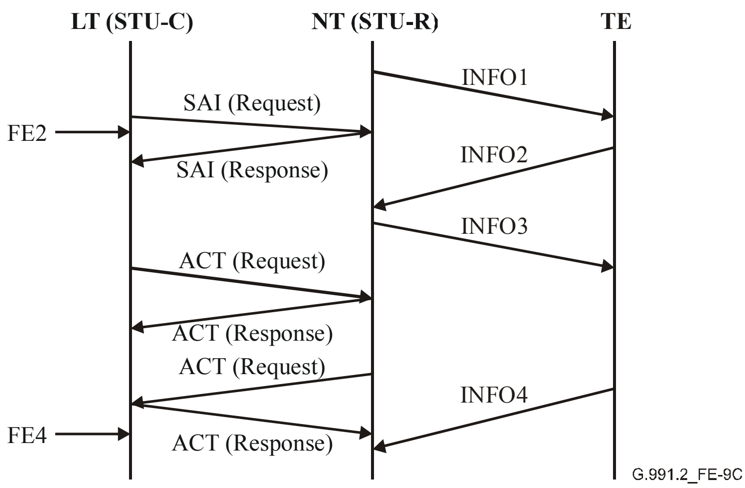


Figure E.9c/G.991.2 – ISDN BA activation initiated by the terminal equipment

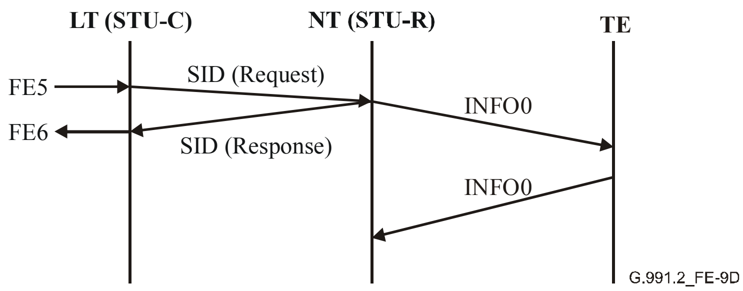


Figure E.9d/G.991.2 – ISDN BA activation initiated by the terminal equipment

Table E.16/G.991.2 – State transition table for the NT

State number	**NT1.1**	**NT1.2**	**NT1.3**	**NT1.4**	**NT1.5**	**NT1.5A**	**NT1.6**	**NT1.7**	**NT1.8**	**NT1.9**	**NT2.0**	**NT2.0A**	**NT2.1**
State name			**ISDN service activation**				**ISDN service activated**				**Loopback 2**		
	Reset	**ISDN service deactivated**	**Initiated**	**T interface activated**	**T interface activated ack**	**Active pending**	**Active**	**LOS/LFA at T pending**	**LOS/LFA at T**	**Deactivation initiated**	**Loopback pending**	**Loopback activate ack**	**Loopback operated**
INFO sent (CP-IWF → TE)	INFO0	INFO0	INFO0	INFO2	INFO2	INFO2	INFO4	INFO2	INFO2	INFO0	INFO2	INFO2	INFO4
Internal state / Event	G1	G1	G1	G2	G2	G2	G3	G2	G2	G4	G4	G4	G4
Receiving INFO0	–	–	–	–	–	–	NT1.7 SDI (Request)	–	–	NT1.2	–	–	–
Receiving INFO1	–	NT1.3 SAI (Request)	–	–	–	–	–	–	–	–	–	–	–
Receiving INFO3	–	–	–	NT1.5 ACT (Request)	–	–	–	–	NT1.5 ACT (Request)	–	NT2.1 ACT (Request)	–	–
LOS/LFA at T	–	–	–	–	–	–	NT1.7 SDI (Request)	–	–	–	–	–	–
SIA (Request)	–	NT1.4 SIA (Response)	–	–	–	–	–		–	NT1.4 SIA (Response)	–	–	–
SAI (Response)	–	–	NT1.4	–	–	–	–	–	–	–	–	–	–
SID (Request)	–	–	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)	–	NT1.9 SID (Response)	NT1.9 SID (Response)	NT1.9 SID (Response)
ACT (Response)		–	–	–	NT1.5	–	–	–	–	–	–	NT2.1	–
ACT (Request)	–	–	–	–	–	NT1.6 ACT (Response)	–	–	–	–	–	–	–

Table E.16/G.991.2 – State transition table for the NT

State number	**NT1.1**	**NT1.2**	**NT1.3**	**NT1.4**	**NT1.5**	**NT1.5A**	**NT1.6**	**NT1.7**	**NT1.8**	**NT1.9**	**NT2.0**	**NT2.0A**	**NT2.1**
State name	**Reset**	**ISDN service deactivated**	**ISDN service activation**				**ISDN service activated**				**Loopback 2**		
			Initiated	**T interface activated**	**T interface activated ack**	**Active pending**	**Active**	**LOS/LFA at T pending**	**LOS/LFA at T**	**Deactivation initiated**	**Loopback pending**	**Loopback activate ack**	**Loopback operated**
Operate 2B+D loopback (Request)	–	NT2.0 Operate 2B+D loopback (success) (Response)	–	–	–	–	–	–	–	–	–	–	–
S reset (Request)	–	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)	NT1.1 S reset ack (Response)
SDI (Response)	–	–	–	–	–	–	–	NT1.8			–		–
SHDSL: $Data_r$ not reached	–	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1	NT1.1
SHDSL: $Data_r$ reached	NT1.2	–	–	–	–	–	–	–	–	–	–		–

Table E.16a/G.991.2 – State transition table for the LT

State number	**LT1.1**	**LT1.2**	**LT1.3**	**LT1.4**	**LT1.5**	**LT1.6**	**LT1.7**	**LT1.8**	**LT2.0**	**LT2.1**	**LT2.2**
State name	**Reset**	**ISDN service deactivated**	**ISDN service activation**			**ISDN service activated**			**Loopback 2**		
			Initiated	**T interface activated**	**Active pending**	**Active**	**LOS/LFA at T**	**Deactivation initiated**	**Loopback requested**	**Loopback pending**	**Loopback operated**
FE sent (CO-IWF → ET) / Event	FE7	FE6	FE2	FE2	FE3	FE4	FE12	(Note)	FE3	FE3	FE4
FE1	–	LT1.3 SIA (Request)		–	–	–	–	LT1.3 SIA (Request)	–	–	–
FE5	–	–	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)	–	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)	Start T2 LT1.8 SID (Request)
FE8	–	LT2.0 Operate 2B+D loopback (Request)			LT2.0 Operate 2B+D loopback (Request)	LT2.0 Operate 2B+D loopback (Request)					
S reset	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1
SAI (Request)	–	LT1.4 SAI (Response)	LT1.3 SAI (Response)	–	–	–	–	–	–	–	–
ACT (Request)	–	–	–	LT1.5 ACT (Response) ACT (Request)	–	–	LT1.5 ACT (Response) ACT (Request)	–	–	LT2.2 ACT (Response)	–
SDI (Request)	–	–	–	–	–	LT1.7 SDI (Response)	–	–	–	–	–
SIA (Response)		–	LT1.4		–	–			–	–	–

Table E.16a/G.991.2 – State transition table for the LT

State number	**LT1.1**	**LT1.2**	**LT1.3**	**LT1.4**	**LT1.5**	**LT1.6**	**LT1.7**	**LT1.8**	**LT2.0**	**LT2.1**	**LT2.2**
State name	**Reset**	**ISDN service deactivated**	**ISDN service activation**			**ISDN service activated**			**Loopback 2**		
			Initiated	**T interface activated**	**Active pending**	**Active**	**LOS/LFA at T**	**Deactivation initiated**	**Loopback requested**	**Loopback pending**	**Loopback operated**
SID (Response)	–	–	–	–	–	–	–	LT1.2	–	–	–
ACT (Response)	–	–	–	–	LT1.6	–		–		–	–
Operate 2B+D loopback (success) (Response)	–	–	–	–	–	–			LT2.1	–	–
S reset ack (Response)	LT1.2	–	–	–	–	–	–		–	–	–
SHDSL: $Data_c$ failed	/	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1	LT1.1
SHDSL: $Data_c$ reached	LT1.2	–	–	–	–	–	–	–	–	–	–
Expiry Timer 2		–	–	–	–	–		LT1.3	–	–	–

Table E.16b/G.991.2 – Legend for the State transition tables

Name	Description
–	No state change
/	Impossible by definition of peer-to-peer physical layer procedures or system internal reasons.
|	Impossible by definition of the physical layer service.
Start T2	Start Timer T2 A description of timer T2 can be found in Note 2 to Table 6 of ETSI ETS 300 012: "Timer 2 (T2) prevents unintentional reactivation. Ist value is 25 ms ≤ value ≤ 100 ms. This implies that the TE has to recognize INFO0 and to react on it within 25 ms. If the NT is able to unambiguously recognize INFO1, then the value of timer 2 may be 0, and an MPH-DEACTIVATE REQUEST would cause a direct transition from state G2 or G3 to G1. It should be noted that the unambiguous detection of INFO1 may not be possible in passive bus configurations, considering all possible implementations."
Note	The FE sent to the network is identical to the FE sent prior to the issue of FE5 from the network.
FE1	(LT ← ET) Activate access
FE2	(LT → ET) Access activation initiated
FE3	(LT → ET) Access digital section activated
FE4	(LT → ET) Access or loopback activated
FE5	(LT ← ET) Deactivate access
FE6	(LT → ET) Access deactivated
FE7	(LT → ET) LOS/LFA in DS or loss of power in NT1
FE8	(LT ← ET) Activate loopback 2
FE12	(LT → ET) LOS/LFA at T reference point

Table E.17/G.991.2 – Reset Request

Message	EOC message code	Comment
S reset	0000 0000	

Table E.18/G.991.2 – Reset Response

Message	EOC message code	Comment
S reset acknowledge	1000 0000	

E.8.10 Transport of ISDN EOC messages over SHDSL EOC

Table E.19 shows the six of the eight codes of the EOC functions which are defined in the ISDN standard. (The two messages concerning the corrupted CRC are not required.)

Table E.19/G.991.2 – ISDN EOC message codes

Message	Message code	Network	STU-R1	REG
Operate 2B + D loopback	0011 0001	o	d	t/d
Operate B1-channel loopback (Note)	0011 0010	o	d	t/d
Operate B2-channel loopback (Note)	0011 0011	o	d	t/d
Return to normal	0011 1111	o	d	t/d
Hold state	0011 0000	d/o	o/d	o/d/t
Origin (o) & destination (d) & transfer (t) NOTE – The use of B1- and B2-channel loopbacks is optional. However, the loopback codes are reserved for these functions.				

E.9 TPS-TC for ATM transport

E.9.1 Definitions

ATM Asynchronous Transfer Mode

HEC Header Error Check

E.9.2 Reference model for ATM transport

The ATM TC layer for SHDSL is consistent with ITU-T Rec. I.432.1 [8]. It shall provide the following functions, as defined in ITU-T Rec. I.432.1:

- Rate decoupling between ATM layer and the synchronous (or plesiochronous) PMS-TC layer.
- Insertion/Extraction[4] of Idle cells.
- Insertion/Extraction[5] of ATM Header Error Check (HEC) byte.
- Cell payload scrambling/descrambling for SDH-based systems.
- Cell delineation in the receive channel.
- Bit timing and ordering (MSB sent first with bit timing synchronous to the STU-C downstream timing base).

The HEC covers the entire cell header. The code used for this function is capable of either:

- single bit error correction; or
- multiple bit error detection.

Error detection shall be implemented as defined in ITU-T Rec. I.432.1 [8] with the exception that any HEC error shall be considered as a multiple bit error, and therefore, HEC error correction shall not be performed.

Figure E.10 shows the logical interface between the ATM Layer, the ATM-TC and the SHDSL PMS-TC function.

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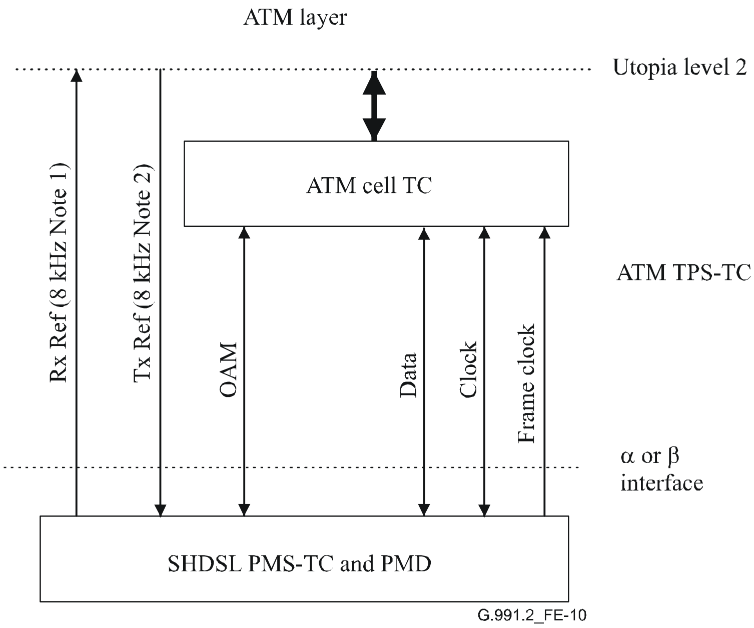
[4] An idle cell inserted at the transmit side has to be extracted at the remote side.

[5] A HEC byte inserted at the transmit side has to be extracted at the remote side.



NOTE 1 – RxRef may be present at the STU-R.
NOTE 2 – TxRef may be present at the STU-C.

Figure E.10/G.991.2 – ATM-TC logical interface to PMS-TC and TPS-TC ATM layer

An ATM Utopia level 2 interface connects the ATM-TC to the ATM Layer. This interface may also be realized logically. Byte boundaries, at the ATM Utopia interface, shall be preserved in the SHDSL payload. Bytes are transmitted MSB first, in accordance with ITU-T Rec. I.432.1 [8].

E.9.2.1 Framing

The PMS-TC provides a clear channel to the ATM-TC and cells are mapped into the SHDSL payload on a byte-by-byte basis. At the STU-C, cells are mapped across the logical α interface while at the STU-R, cells cross the logical β interface, as identified in 4.1. At the α and β interface, logical data and clock lines are present. Cell alignment to the frame is optional. The ATM stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing n 8-bit time slots. Each byte from the input ATM data stream is mapped MSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot n. A total of k_s bits (or n bytes) of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \leq n \leq 36$. Note that optional extensions described in Annex F allow values of n up to 89. See Figure E.10a for additional details.

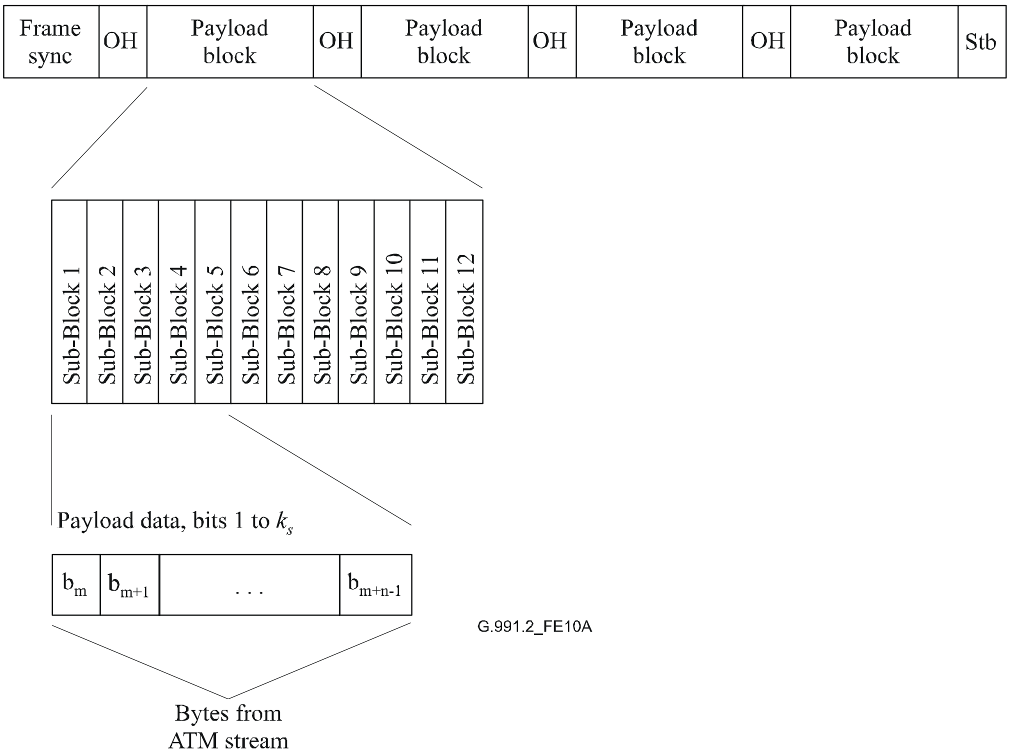


Figure E.10a/G.991.2 – ATM framing

In the optional *M*-pair mode, ATM data is carried over all pairs using interleaving, as described in 8.2. In *M*-pair mode only multiples of *M* time slots may be supported. The input ATM stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing $M \times n$ 8-bit time slots. Each byte from the input ATM data stream is mapped MSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot *n*. A total of $M \times k_s$ bits (or $M \times n$ bytes) of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Note that optional extensions described in Annex F allow values of *n* up to 89. The bytes from the input ATM data stream shall be interleaved among all *M* pairs, such, where byte b_m is carried on Pair *m*, byte b_{m+1} is carried in the corresponding time slot on Pair $m + 1$. Thus, pair *M* carries the *m*th time slot out of every block of *M* time slots. See Figure E.10b for additional details.

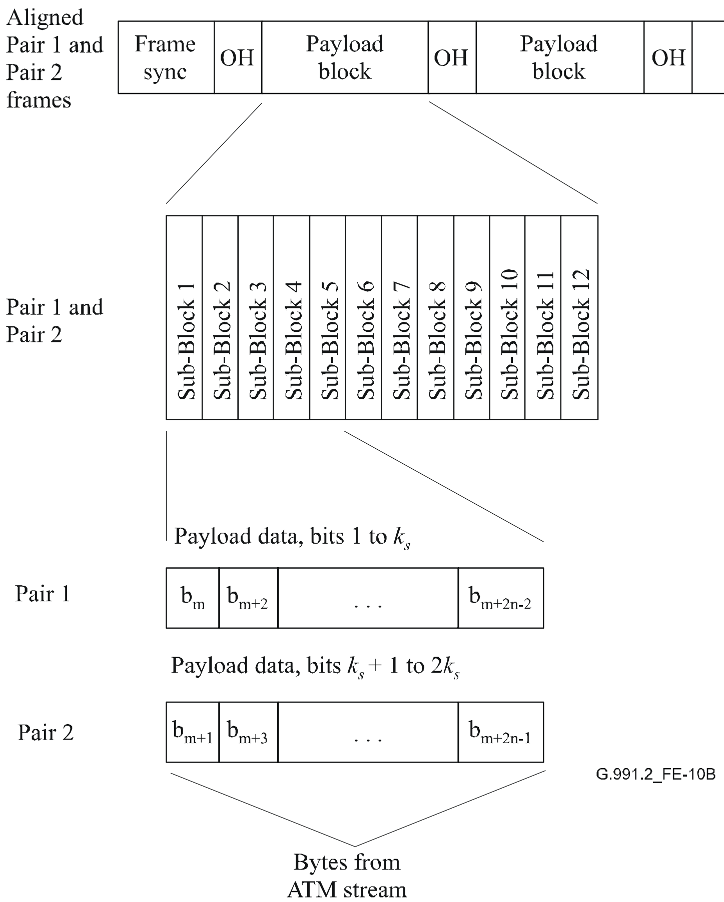


Figure E.10b/G.991.2 – *M*-pair framing for ATM (for the *M* = 2 case)

E.9.2.2 Timing

STUs shall be operated in either synchronous or plesiochronous mode; however, in most applications synchronous operation is preferred. In either case, the STU-C frame clock is locked to network timing.

The provision of Network Timing Reference from the STU-C to the STU-R for ATM is optional; however, if an NTR is provided, the SHDSL PMS-TC shall operate in clock synchronization mode 3a (see 10.1). The network timing reference shall be an 8 kHz marker from which clocks at other frequencies could easily be derived. In this clock mode, both the frame and symbol clocks at the STU-C are locked to the NTR. The STU-R may extract the NTR from the received Frame Synchronization Word (FSW). Referring to Figure E.10, the TxRef (in the STU-C) lines carries NTR directly to the PMS-TC, while RxRef (in the STU-R) carries the NTR to the ATM Layer from PMS-TC. Synchronization to the NTR shall be as described in 10.4.

E.9.2.3 IMA using the ATM TPS-TC (Informative)

The ATM TPS-TC, as defined in E.9, is intended to be compatible with Inverse Multiplexing for ATM (IMA) Specification, as defined in af-phy-0086.001 [B12]. IMA is a protocol that provides for inverse multiplexing of an ATM cell stream over multiple physical layer transmission links. It operates by multiplexing the ATM cell stream between the links on a cell-by-cell basis and then inserting special IMA Control Protocol (ICP) cells into each of the individual ATM cell streams. Since the IMA cell stream for each link is structurally identical to a stream of normal ATM cells, IMA cell streams may be carried without modification using the SHDSL ATM TPS-TC. Note that the IMA Specification assumes that the ATM TPS-TC will be compatible with the IMA exceptions to the Interface Specific Transmission Convergence Sublayer, as defined in the IMA Specification, 5.2.1 (specifically, items R-3 and R-4).

The IMA Specification (9.1) indicates that the differential delay from the IMA transmitter to the loop interface (U-R or U-C) is to be no greater than 2.5 cells. Clause 7.1.6 recommends a maximum differential signal transfer delay between non-repeatered SHDSL wire pairs of no more than 50 µs at 150 kHz. With regard to repeaters, note that this Recommendation (9.5.5.5) allows up to 8 repeaters in an access link; however, it does not define the delay though the repeater. Also note that the number of repeaters deployed in a loop is dependent on network-specific conditions. Implementers are encouraged to take into account the various sources of differential delay, including differential latencies introduced by repeaters (if present), in the design of IMA systems.

E.9.3 Transport capacity and flow control

An STU transporting ATM shall support N × 64 kbit/s data rates. The payload data rate shall be: $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $i = 0$. This restriction applies to the data rate and payload block size, as specified in 7.1.1, 8.1 and 8.2. Note that optional extensions described in Annex F allow values of n up to 89.

In the optional *M*-pair mode, the rates specified shall apply per pair.

The ATM-TC shall provide flow control, allowing the STU-C and STU-R to control the cell flow from the ATM layer. This functionality is implemented through the TX_Cell Handshake and RX_Cell handshake at the ATM Utopia bus interface. A cell may be transferred to the ATM-TC layer only after the completion of a TX_Cell Handshake. Similarly, a cell may be transferred from the ATM-TC to the ATM Layer only after the STU has completed an RX_Cell_Handshake. This functionality is important to avoid cell overflow and underflow at the TU layer.

E.9.4 Operations and maintenance

The ATM-TC requires Operations, Administration and Maintenance (OAM) functionality. The messaging protocol and format should be handled in accordance with clause 9. The OAM functions notify the OAM entity at the opposite end of the line upon the status of the cell delineation process (e.g., Header Error Check (HEC) anomalies and Loss of Cell Delineation defects (LCD)). Performance parameters are derived from anomalies and defects.

E.9.4.1 ATM data path related near-end anomalies

Near-end No Cell Delineation (nncd) anomaly: An *nncd* anomaly occurs immediately after ATM-TC start-up, when ATM data is received and the cell delineation process is in HUNT or PRESYNC state. Once cell delineation is acquired, subsequent losses of cell delineation shall be considered *nocd* anomalies.

Near-end Out of Cell Delineation (nocd) anomaly: An *nocd* anomaly occurs when the cell delineation process in operation transitions from the SYNC state to HUNT state. An *nocd* anomaly terminates when the cell delineation process transition from PRESYNC to SYNC state or when *nlcd* defect maintenance status is entered.

Near-end Header Error Control (nhec) anomaly: An *nhec* anomaly occurs when an ATM cell header error control fails.

E.9.4.2 ATM data path related near-end defects

Near-end Loss of Cell Delineation (nlcd) defect: An *nlcd* defect occurs when at least one *nocd* is present in 9 consecutive SHDSL frames and no *losw* defect (loss of synchronization word) is detected. An *nlcd* defect terminates after the cell delineation process has entered and remained in the SYNC state in 9 consecutive SHDSL frames.

E.9.4.3 ATM data path related far-end anomalies

Far-end No Cell Delineation (fncd) anomaly: An *fncd* anomaly is an *nncd* anomaly that is reported from the far end by the NCD indicator in the EOC ATM Cell Status Information message. An *fncd* anomaly occurs immediately after start-up and terminates if the received NCD indicator is coded 0.

Note that, since the far end reports the NCD indicator only on request, the *fncd* anomaly may be inaccurate for derivation of the far-end NCD failure. Therefore, the NCD failure is autonomously reported from the far end.

Far-end Out of Cell Delineation (focd) anomaly: A *focd* anomaly is a *nocd* anomaly, that is reported from the far end by the OCD indicator in the EOC ATM Cell Status Information message. The OCD indicator shall be coded 0 to indicate no *nocd* anomaly has occurred since last reporting and shall be coded 1 to indicate that at least one *nocd* anomaly has occurred since last reporting. An *focd* anomaly occurs if no *fncd* anomaly is present and a received OCD indicator is coded 1. An *focd* anomaly terminates if a received OCD indicator is coded 0.

Far-end Header Error Control (fhec) anomaly: An *fhec* anomaly is an *nhec* anomaly, that is reported from the far end by the HEC indicator in the EOC ATM Cell Status Information message. The HEC indicator shall be coded 0 to indicate no *nhec* anomaly has occurred since last reporting and shall be coded 1 to indicate that at least one *nhec* anomaly has occurred since last reporting. An *fhec* anomaly occurs if a received HEC indicator is coded 1. An *fhec* anomaly terminates if a received HEC indicator is coded 0.

E.9.4.4 ATM data path related far-end defects

Far-end Loss of Cell Delineation (flcd) defect: An *flcd* defect is an *nlcd* that is reported from the far end of the line by the LCD indicator in the EOC ATM Cell Status Information message. The LCD indicator shall be coded 0 to indicate no *nlcd* defect has occurred since last reporting and shall be coded 1 to indicate that at least one *nlcd* defect has occurred since last reporting. An *flcd* defect occurs when the LCD indicator is coded 1. An *flcd* defect terminates when the LCD indicator is coded 0.

Note that, since the far end reports the LCD indicator only on request, the *flcd* defect may be inaccurate for derivation of the far-end LCD failure. Therefore, the LCD failure is autonomously reported from the far end.

E.9.4.5 ATM cell level protocol performance information collection

HEC violation count (hvc): An *hvc* performance parameter is the count of the number of *nhec* anomalies modulo 65536.

HEC total count (htc): An *htc* performance parameter is the count of the total number of cells passed through the cell delineation process, while operating in the SYNC state, since the last reporting.

These values shall be counted, such that the Management system is able to retrieve current counts on a 15-minute and 24-hour basis.

E.9.4.6 Failures and performance parameters

nncd failures and *nlcd* failures relate to persistent *nncd* anomalies and persistent *nlcd* defects, respectively. The definitions below are derived from 7.1.2/G.997.1 [3]. These failures are reported in the ATM Cell Status Information message.

E.9.4.6.1 ATM data path related near-end failures

The following near-end failure indications shall be provided by the STU-C and the STU-R:

E.9.4.6.1.1 Near-End No Cell Delineation (*nncd*) failure

An *nncd* failure is declared when an *nncd* anomaly persists for more than 2.5 ± 0.5 s after the start of Data Mode. An *nncd* failure terminates when no *nncd* anomaly is present for more than 10 ± 0.5 s.

E.9.4.6.1.2 Near-End Loss of Cell Delineation (*nlcd*) failure

An *nlcd* failure is declared when an *nlcd* defect persists for more than 2.5 ± 0.5 s. An *nlcd* failure terminates when no *nlcd* defect is present for more than 10 ± 0.5 s.

E.9.4.6.2 ATM data path related far-end failures

The following far-end failure indications shall be provided at the STU-C (the STU-R is at the far end), and are optional at the STU-R (the STU-C is at the far end).

E.9.4.6.2.1 Far-End No Cell Delineation (*fncd*) failure

An *fncd* failure is declared when an *fncd* anomaly persists for more than 2.5 ± 0.5 s after the start of Data Mode. An *fncd* failure terminates when no *fncd* anomaly is present for more than 10 ± 0.5 s.

E.9.4.6.2.2 Far-End Loss of Cell Delineation (*flcd*) failure

An *flcd* failure is declared when an *flcd* defect persists for more than 2.5 ± 0.5 s. An *flcd* failure terminates when no *flcd* defect is present for more than 10 ± 0.5 s.

E.9.4.7 EOC ATM Cell Status Request message format – Message ID 17

The ATM Cell Status Request/Confirmation message is used for two purposes. This message is used as ATM Cell Status Request message to get the STU-R ATM Status. For this purpose, the whole information of EOC ATM Cell Status Information message – Message ID 145 shall be sent in response to this message. If an unexpected receipt of ATM Cell Status message – Message ID 145 is received including NCD or LCD failure indication, this message may be used to confirm the reception and stop future autonomous transmission of the ATM Cell Status message – Message ID 145 due to the current failure condition.

Table E.20/G.991.2 – ATM Cell Status Request information field

Octet #	Information field	Data type
1	Message ID 17	Message ID

E.9.4.8 EOC ATM Cell Status Information message format – Message ID 145

The ATM Cell Status Information message shall be sent in response to the ATM Cell Status Request message and shall be sent autonomously upon the occurrence of an *nlcd* Failure or an *nncd* Failure. Table E.21 shows the OAM message bit encoding for an ATM Cell Status Information message. The HEC Indicator is implicitly defined as set to 1 if the HEC violation count has changed since last reporting and set to 0 otherwise. If sent autonomously, Message ID 145 is sent once every second until a Message ID 17 is received from the STU-C or the failure is cleared.

The NCD, OCD, and LCD Indicator bits shall indicate the state of *nncd* anomaly, *nocd* anomaly, and *nlcd* defect, respectively. NCD Failure and LCD Failure bits shall serve as indications of *nncd* failure and *nlcd* failure, respectively.

Table E.21/G.991.2 – ATM cell status information message

Octet #	Contents	Data type	Reference
1	Message ID 145	Message ID	
2, bit 7	NCD Indicator (Note)	Bit	0 = OK, 1 = alarm
2, bit 6	OCD Indicator (Note)	Bit	0 = OK, 1 = alarm
2, bit 5	LCD Indicator (Note)	Bit	0 = OK, 1 = alarm
2, bits 4-2	Reserved		
2, bit 1	NCD Failure	Bit	0 = OK, 1 = alarm
2, bit 0	LCD Failure	Bit	0 = OK, 1 = alarm
3	HEC violation count (*hvc*)	MS Byte	16-bit counter, modulo 65536
4	HEC violation count (*hvc*)	LS Byte	16-bit counter, modulo 65536
NOTE – Only one of the NCD, OCD, and LCD Indicators can be set to 1 at any time.			

E.10 Dual-bearer TPS-TC mode

The TPS-TC modes in E.1 through E.9 and E.11 through E.13 are described as operating in Single-Bearer Mode; i.e., the payload is treated as a single data stream, and the TPS-TC uses all of the bits in each Payload Sub-Block. In some applications, however, it is desirable to split the payload into separate data streams supporting multiple user interfaces or different data types. Dual-Bearer Mode provides support for these cases.

Support for Dual-Bearer Mode is optional, as is support for each of the Dual-Bearer TPS-TC combinations specified in Table E.22.

In Dual-Bearer Mode, each Payload Sub-Block is split between two separate TPS-TC instances. The TPS-TC modes are negotiated independently in ITU-T Rec. G.994.1, and there is no direct interaction between them. TPS-TC_a is assigned the first k_{sa} bits of each Payload Sub-Block, and TPS-TC_b is assigned the last k_{sb} bits of each Payload Sub-Block (see Figure E.11). For each of the two TPS-TCs, the k_s bits assigned to it are treated as if they constituted a complete Payload Sub-Block, and appropriate framing is applied, as described in E.1 to E.9 and E.11 to E.13 associated with the selected TPS-TC.

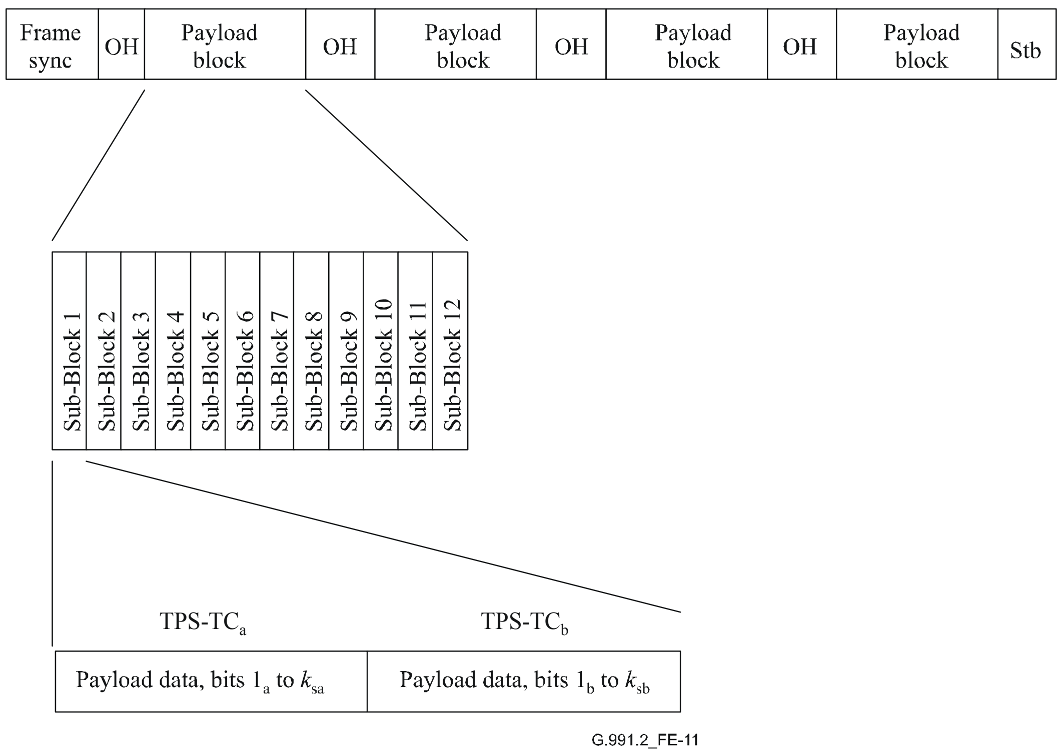


Figure E.11/G.991.2 – Dual-bearer mode TPS-TC framing

Figure E.12 shows an example of a Dual-Bearer mode in which Fractional DS1 is TPS-TC$_a$ and ATM is TPS-TC$_b$.

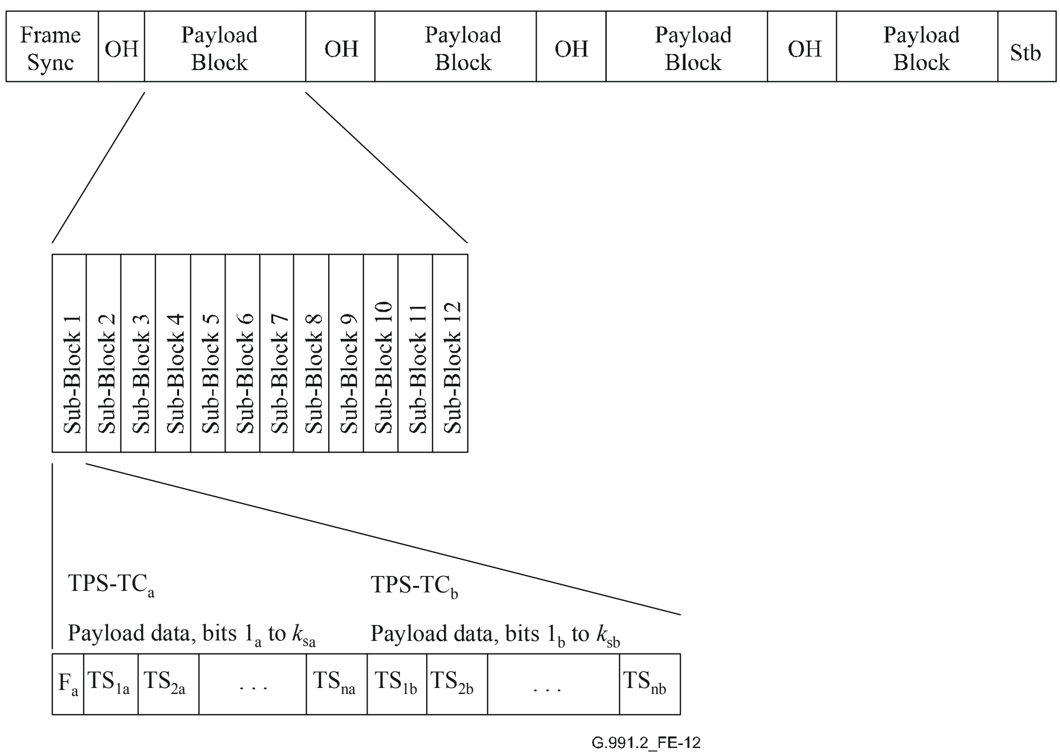


Figure E.12/G.991.2 – Example of dual-bearer mode TPS-TC framing

In the optional *M*-pair mode, the same procedure is followed for Dual-Bearer Mode. The first k_{sa} bits on each pair are assigned to TPS-TC_a, and the last k_{sb} bits on each pair are assigned to TPS-TC_b. The appropriate *M*-pair TPS-TC framing is then applied, as described in E.1 through E.9 and E.11 through E.13.

E.10.1 Dual-bearer clock synchronization

In Dual-Bearer Mode, it is assumed that timing for the two Bearer Channels is derived from a common source and that the two data streams thus have a definite clocking relationship. As such, no mechanism is provided within the payload blocks to maintain synchronization between the Bearer Channels, regardless of the clock mode that is selected (10.1).

Note that some TPS-TCs have limitations on the clock modes that are supported. Specifically, ATM using NTR (E.9.2) and Synchronous ISDN BA (E.8) are only defined for Clock Mode 3a (see 10.1). When either of these TPS-TCs is used as part of a Dual-Bearer Mode, the system shall operate in Clock Mode 3a.

E.10.2 Dual-bearer mode types

The following three types of dual-bearer modes are supported within SHDSL:

Type 1 – STM + Broadband.

Type 2 – STM + Cell/Packet.

Type 3 – STM + Clear Channel.

For each type of dual-bearer mode, separate specification bits are provided within ITU-T Rec. G.994.1 for the selection of the two TPS-TCs to be used. Table E.22 lists the combinations that are supported. Other supported types are for further study.

Table E.22/G.991.2 – Supported TPS-TCs in dual-bearer mode

Type	Description	TPS-TC_a	TPS-TC_b
1	STM + Broadband	Synchronous ISDN BA (E.8) LAPV5 Enveloped POTS or ISDN (E.13) (Note 2) STM with DSC (E.12)	Clear Channel (E.1) Clear Channel Byte-Oriented (E.2) Unaligned DS1 (E.3) (Note 1) Aligned DS1/Fractional DS1 (E.4) (Note 1) Unaligned D2048U (E.5) (Note 2) Unaligned D2048S (E.6) (Note 2) Aligned D2048S/Fractional D2048S (E.7) (Note 2) ATM (E.9) PTM (E.11)
2	STM + Cell/Packet	Unaligned DS1 (E.3) (Note 1) Aligned DS1/Fractional DS1 (E.4) (Note 1) Unaligned D2048U (E.5) (Note 2) Unaligned D2048S (E.6) (Note 2) Aligned D2048S/Fractional D2048S (E.7) (Note 2)	ATM (E.9) PTM (E.11)

Table E.22/G.991.2 – Supported TPS-TCs in dual-bearer mode

Type	Description	TPS-TC$_a$	TPS-TC$_b$
3	STM + Clear Channel	Unaligned DS1 (E.3) (Note 1) Aligned DS1/Fractional DS1 (E.4) (Note 1) Unaligned D2048U (E.5) (Note 2) Unaligned D2048S (E.6) (Note 2) Aligned D2048S/Fractional D2048S (E.7) (Note 2)	Clear Channel (E.1) Clear Channel Byte-Oriented (E.2)
NOTE 1 – Denotes TPS-TC modes that typically apply only in North American networks. NOTE 2 – Denotes TPS-TC modes that typically apply only in European networks.			

E.10.3 Dynamic rate repartitioning

Dynamic Rate Repartitioning (DRR) is the procedure for temporarily allocating time slots between the STM Bearer and the Broadband Bearer. The DRR protocol is a master/slave protocol based on messaging, at a rate of one message per superframe. Either the STU-C or the STU-R may be the DRR master; this is configured through ITU-T Rec. G.994.1 [2] during pre-activation. The DRR protocol will be triggered and controlled by a higher layer management entity, denoted in this clause as a supervisory entity.

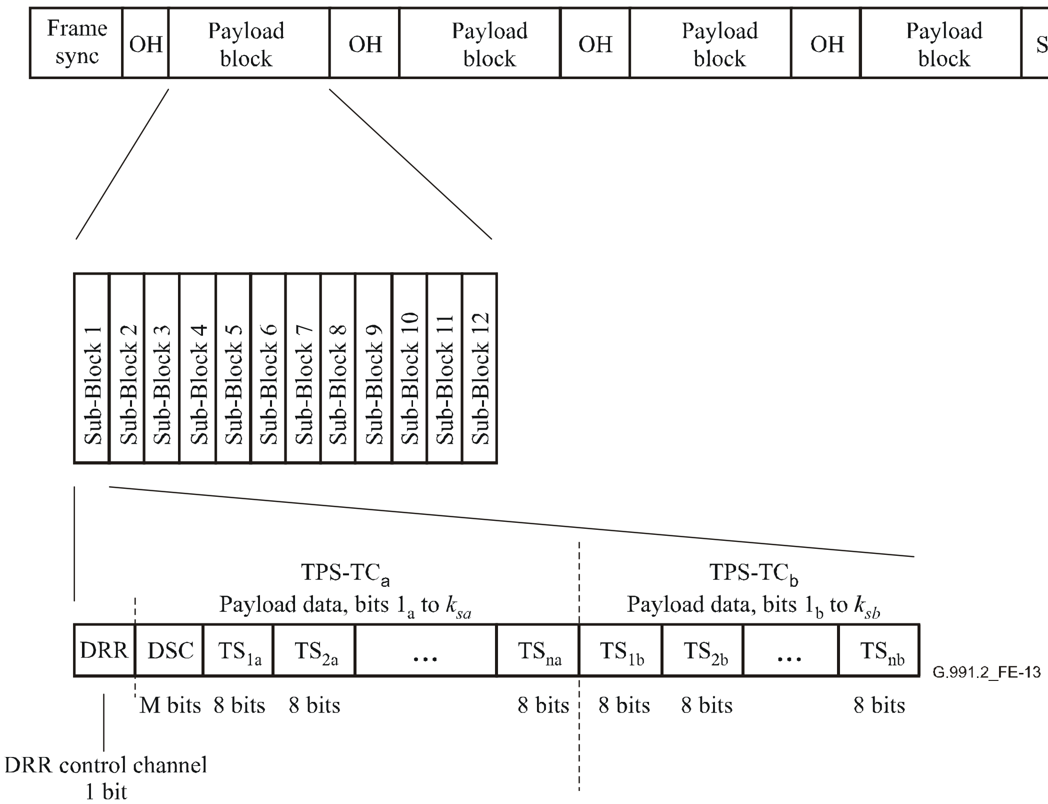


Figure E.13/G.991.2 – Dual-bearer mode framing with DRR

Figure E.13 shows an example of a dual-bearer mode with a dedicated DRR control channel, for transport of the DRR protocol messages. These messages control the activation and de-activation of time slots in the STM Bearer, and the corresponding de-allocation/allocation to the Broadband Bearer. The Dedicated Signalling Channel (DSC) carries signalling information for telephony. Its bandwidth depends on the application, and can be 0. This example shows 1 bit dedicated to DRR in each Sub-Block, which corresponds to 8 kbit/s capacity. Adding more DRR bits increases the capacity of the DRR control channel.

E.10.3.1 Message structure

The DRR message structure is shown in Figure E.14. These messages will be sent between the DRR master and the DRR slave. The messages consist of one leading Control octet, followed by Channel-ID octet(s). There is one Channel-ID octet for every 8 time slots to be managed by the DRR procedure. The Control octet has 4 bits for the message type, followed by 4 bits for the sequence number. Each bit of the Channel-ID octets corresponds to one time slot, the time slots following, in the frame, the same order as the Channel-ID bits:

– "1": The corresponding time slot is currently active as part of the STM bearer channel, or is in the process of being activated.

– "0": The corresponding time slot is not in use, and is thus available for broadband data.

Octet #1 (Control)		**Octet #2 (Channel ID)**		**Octet #3 (Channel ID)**		**Octet #4 (Channel ID)**	
b b b b	b b b b	b b b b	b b b b	b b b b	b b b b	b b b b	b b b b
Message type	Sequence No.	1 2 3 4 Time slots	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24

Figure E.14/G.991.2 – DRR message structure

NOTE – This example assumes the SHDSL system is managing 24 time slots under DRR.

Each message has a sequence number that is used to control the DRR protocol. The exact usage is given in the description of each state; however, in general it serves to indicate either how many times a particular message has been sent in a sequence; or, in a responding message, to which message number it is responding. Particularly, in an environment in which line disturbance can cause protocol delays, the sequence number can be used to ensure synchronization of framing change.

The complete set of DRR messages is shown in Table E.23.

Table E.23/G.991.2 – Messages used in DRR protocol

DRR message type	Code	Direction
MONITOR	1111	Master-to-Slave, Slave-to-Master
DEMAND	1110	Master-to-Slave
DEMAND ACK	1101	Slave-to-Master
DEMAND NAK	1011	Slave-to-Master
EXEC	0001	Master-to-Slave
EXEC ACK	0100	Slave-to-Master
REQUEST	1100	Slave-to-Master

E.10.3.2 Message flow for DRR

Figure E.15 shows a typical message flow for a DRR event.

Downstream				Upstream		
Message sent by Master	**Sequence No.**	**Message received by Slave**		**Message sent by Slave**	**Sequence No.**	**Message received by Master**
Monitor	<0>	Monitor		Monitor	<0>	Monitor
Demand	<1>	Demand		Monitor	<0>	Monitor
Demand	<2>	Demand		Demand Ack	<1>	Demand Ack
Demand	<3>	Demand		Demand Ack	<1>	Demand Ack
Exec	<1>	Exec		Demand Ack	<1>	Demand Ack
Exec	<2>	Exec		Exec Ack	<1>	Exec Ack
Exec	<3>	Exec		Exec Ack	<2>	Exec Ack
Monitor	<0>	Monitor		Exec Ack	<3>	Exec Ack
Monitor	<0>	Monitor		Monitor	<0>	Monitor
Monitor	<0>	Monitor		Monitor	<0>	Monitor
NOTE – Shading change indicates change of framing.						

Figure E.15/G.991.2 – Message flow, assuming STU-C is DRR Master, j = 2

E.10.3.3 Error protection

Each DRR message is stated 3 times within the same SHDSL superframe, and the correct message is determined by a 2-out-of-3 majority decision at the recipient's end.

E.10.3.4 DRR control channel

The DRR messages are carried by a DRR control channel, a dedicated channel made up of one or more Z-bits (8 kbit/s channel). Each Z-bit provides 48 bits (6 octets) per superframe. Since each message is sent 3 times in the same superframe, each Z-bit provides for 2 octets of message. A 1 Z-bit channel can manage up to 8 time slots, while a 2 Z-bit channel, with 4 octets of message, can manage up to 24 time slots. Messages sent from the DRR master to the DRR slave are referred to as "downstream", and messages from the DRR slave to the DRR master are referred to as "upstream". The number of Z-bits to be used must be configured during pre-activation through ITU-T Rec. G.994.1 [2]. Channel-ID bits that are in excess of the number of managed time slots will not be used.

E.10.3.5 Lead time

The lead time *j* used in the countdown is the number of downstream superframes starting with EXEC <1> and ending just before the first downstream superframe with the new framing. This will be the same as the number of upstream superframes starting with EXEC ACK <1> and ending just before the first upstream superframe with the new framing. The value of *j* is to be negotiated during pre-activation through ITU-T Rec. G.994.1 [2].

E.10.3.6 The DRR Protocol – Finite state machine description

The state diagrams for master and slave are given in Figures E.16 and E.17, respectively. The states are shown as bubbles. The name of the state is given in the upper half of the bubble in *italic* font. The message which is transmitted during the state is given in the lower half of the bubble in CAPITAL letters. Incoming messages which trigger state transition are given in CAPITAL letters as well. Information, commands and notifications to/from the supervisory entity are <u>underlined</u>. Logical operation (i.e., **and**, **or**) are given in **bold** letters as well. These rules also apply to the textual description. Notifications to/from the supervisory entity are primitives and are used for illustrative purposes only. Supervisory actions are out of the scope of this Recommendation.

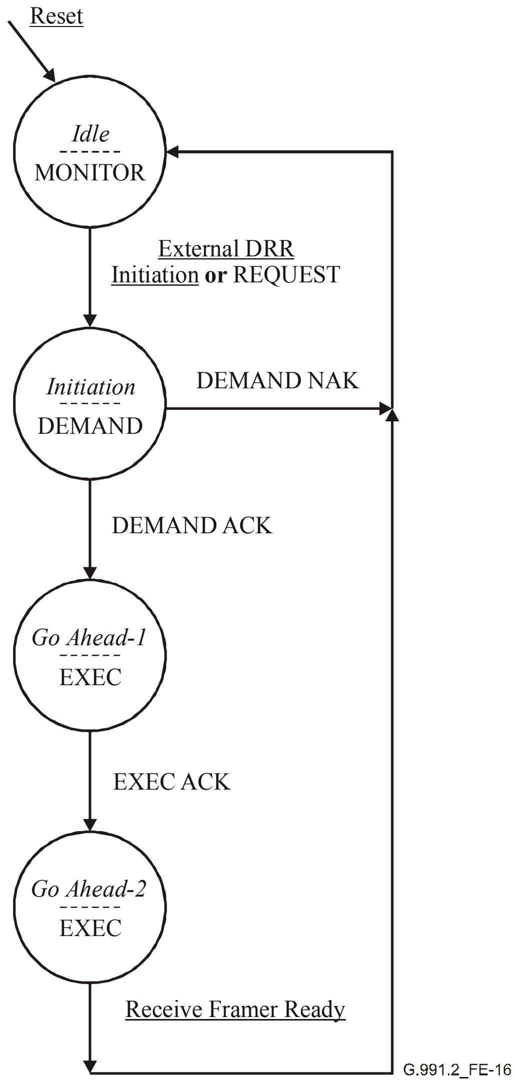


Figure E.16/G.991.2 – State diagram of the master, showing state, outgoing message and trigger conditions

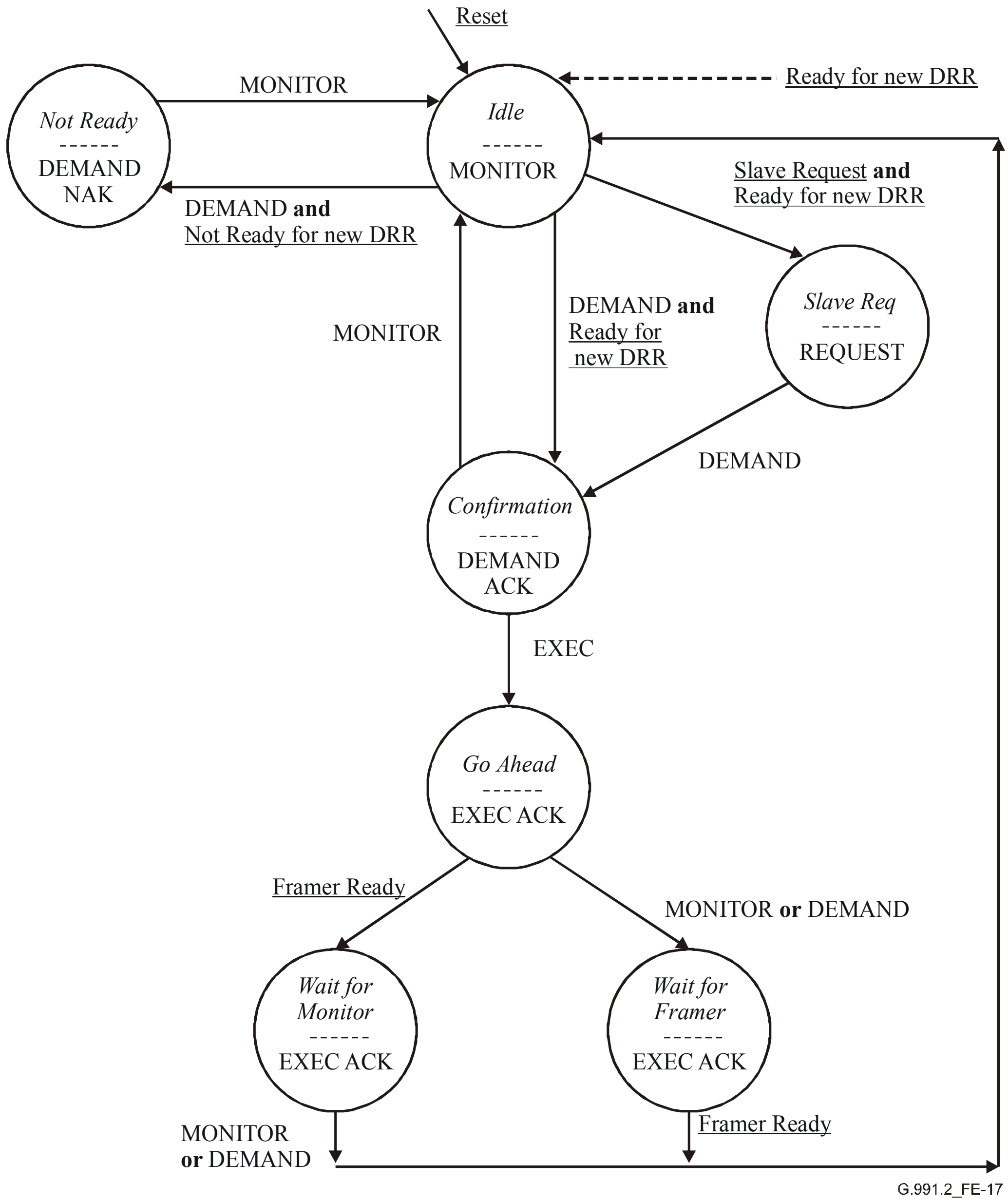


Figure E.17/G.991.2 – State diagram of the slave, showing state, outgoing message and trigger conditions

E.10.3.7 DRR Master state machine

Table E.24/G.991.2 – *Idle* state of the Master

Entrance:		
From state	**Trigger condition**	
Any	Reset from supervisory entity	
Go Ahead-2	Receiver Framer Ready from master	
Initiation	DEMAND NAK	
Action:		
Transmission of MONITOR <0>		
Exit:		
Trigger conditions	**Target state**	**Notification**
External DRR initiation, **or** REQUEST	*Initiation*	

Fail-safe precaution: In the event of a mismatch in the time-slot settings in the Channel-ID octets of the MONITOR upstream and downstream messages, the notification Time-Slot Alarm is issued.

Table E.25/G.991.2 – *Initiation* state of the Master

Entrance:		
From state	**Trigger condition**	
Idle	External DRR initiation, **or** REQUEST	
	+	
Action:		
Transmission of DEMAND <n_D>	n_D begins with 1, and increments until the first trigger condition.	
Exit:		
Trigger conditions	**Target state**	**Notification**
DEMAND ACK	*Go Ahead-1*	Initiation of Transmit Framer
DEMAND NAK	*Idle*	Slave not ready for DRR

Fail-safe precaution: If n_D reaches 15, it no longer increments. This could happen if recognition of DEMAND ACK or DEMAND NAK is delayed, due to disturbance on the line. The notification Sequence Number Overflow is issued, and the message DEMAND <15> continues to be transmitted. The master stays in this state until a valid slave response is received, unless there is supervisory intervention.

Table E.26/G.991.2 – *Go Ahead-1* state of the Master

Entrance:		
From state	**Trigger condition**	
Initiation	DEMAND ACK	
Action:		
Transmission of EXEC $\langle n_E \rangle$	n_E begins with 1, and increments until the first trigger condition.	
Exit:		
Trigger condition	**Target state**	**Notification**
EXEC ACK	*Go Ahead-2*	Initiation of Receiver Framer

Fail-safe precaution: If n_E reaches 15, it no longer increments. This could happen if recognition of the first EXEC ACK is delayed, due to disturbance on the line. The notification Sequence Number Overflow is issued, and the message EXEC <15> continues to be transmitted. The master stays in this state until a valid slave response is received, unless there is supervisory intervention.

Table E.27/G.991.2 – *Go Ahead-2* state of the Master

Entrance:		
From state	**Trigger condition**	
Go Ahead State-1	EXEC ACK	
Action:		
Transmission of EXEC $\langle n_E \rangle$	n_E is fixed at the value it had when exiting *Go Ahead-1* State.	
Exit:		
Trigger condition	**Target state**	**Notification**
Receive Framer Ready	*Idle*	DRR complete

E.10.3.8 DRR Slave state machine

An upper-layer supervisory entity also controls the DRR procedure at the DRR slave side. This entity continually asserts a notification, stating whether the slave is ready to accept a new DRR or not (Ready for new DRR, Not Ready for new DRR).

Table E.28/G.991.2 – *Idle* state of the Slave

Entrance:		
From state	**Trigger condition**	
Any	Reset from supervisory entity	
Confirmation	MONITOR	
Not Ready	MONITOR	
Wait for Monitor	MONITOR, or DEMAND	
Wait for Framer	Framer Ready	
Action:		
Transmission of MONITOR <0>		
Exit:		
Trigger condition	**Target state**	**Notification**
DEMAND **and** Ready for new DRR	*Confirmation*	
Slave Request **and** Ready for new DRR	*Slave Request*	
DEMAND **and** Not Ready for new DRR	*Not Ready*	

Table E.29/G.991.2 – *Slave Request* state of the Slave

Entrance:		
From state	**Trigger condition**	
Idle	Slave Request **and** Ready for new DRR	
Action:		
Transmission of REQUEST <n_R>	n_R begins with 1, and increments until the first trigger condition.	
Exit:		
Trigger condition	**Target state**	**Notification**
DEMAND	*Confirmation*	
NOTE – In applications with tight timing requirements, it is recommended that the *Slave Request* State not be used. Instead, the system should be configured with the Dedicated Signalling Channel (DSC, see E.10.3) to allow normal telephony signalling to inform the master of the need for a DRR.		

Table E.30/G.991.2 – *Confirmation* state of the Slave

Entrance:		
From state	**Trigger condition**	
Idle	DEMAND <n_D> **and** Ready for new DRR	
Slave Request	DEMAND <n_D>	
Action:		
Transmission of DEMAND ACK <n_{DA}>	n_{DA} is fixed at the sequence number n_D of the triggering DEMAND.	
Exit:		
Trigger condition	**Target state**	**Notifications**
EXEC	*Go Ahead*	Send both: – Initiation of Receive and Transmit Framer – Sequence Number of First Received EXEC (for synchronization purposes)

Table E.31/G.991.2 – *Not Ready* state of the Slave

Entrance:		
From state	**Trigger condition**	
Idle	DEMAND <n_D> **and** Not Ready for new DRR	
Action:		
Transmission of DEMAND NAK <n_{DN}>	n_{DN} is fixed at the sequence number n_D of the triggering DEMAND	
Exit:		
Trigger condition	**Target state**	**Notification**
MONITOR	*Idle*	DRR aborted

Table E.32/G.991.2 – *Go Ahead* state of the Slave

Entrance:		
From state	**Trigger condition**	
Confirmation	EXEC	
Action:		
Transmission of EXEC ACK <n_{EA}>	n_{EA} begins with 1, and increments until the first trigger condition.	
Exit:		
Trigger condition	**Target state**	**Notification**
Framer Ready	*Wait for Monitor*	
MONITOR, or DEMAND	*Wait for Framer*	

Fail-safe precaution: If n_{EA} reaches 15, it no longer increments. This could happen if recognition of the first MONITOR or DEMAND is delayed, due to disturbance on the line. The notification Sequence Number Overflow is issued, and the message EXEC ACK <15> continues to be transmitted. The slave stays in this state until a valid master message is received, unless there is supervisory intervention.

Table E.33/G.991.2 – *Wait for Monitor* state of the Slave

Entrance:		
From state	**Trigger condition**	
Go Ahead	Framer Ready	
Action:		
Transmission of EXEC ACK <n_{EA}>	n_{EA} is fixed at the value it had when exiting *Go Ahead* State.	
Exit:		
Trigger condition	**Target state**	**Notification**
MONITOR, or DEMAND	*Idle*	DRR complete

Table E.34/G.991.2 – *Wait for Framer* state of the Slave

Entrance:		
From state	**Trigger condition**	
Go Ahead	MONITOR, **or** DEMAND	
Action:		
Transmission of EXEC ACK <n_{EA}>	n_{EA} is fixed at the value it had when exiting *Go Ahead* State.	
Exit:		
Trigger condition	**Target state**	**Notification**
Framer Ready	*Idle*	DRR complete

E.10.3.9 Result of DRR procedure

Figure E.11 shows the TPS-TC framing for the Dual-Bearer mode. Figure E.18 demonstrates how the mapping of the payload sub-block will be changed by the DRR procedure, in a typical application example. In the initial configuration of this example, the eight 8-bit time slots TS_{xa} that belong to TPC-TC_a carry STM (voice) and the n 8-bit time slots TS_{xb} that belong to TPS-TC_b carry ATM. When the supervisory entity recognizes that time slot TS_{2a} is not currently carrying voice samples, it instigates a DRR procedure which temporarily repartitions TS_{2a} to the ATM bearer: then seven time slots are carrying STM data, and (n + 1) are carrying ATM data.

Also shown is the DRR control channel and the Dedicated Signalling Channel (DSC) in Figure E.18. In this example, the DRR control channel uses only 1 Z-bit, which is enough to manage eight time slots (see E.10.3.4). The Dedicated Signalling Channel (DSC) carries the higher-layer telephony signalling for the STM time slots (e.g., per Telcordia GR-303 [B14] or ETSI V5 [9] & [B16]); in applications using channel associated signalling (CAS), and without tight timing constraints, the DSC is optional.

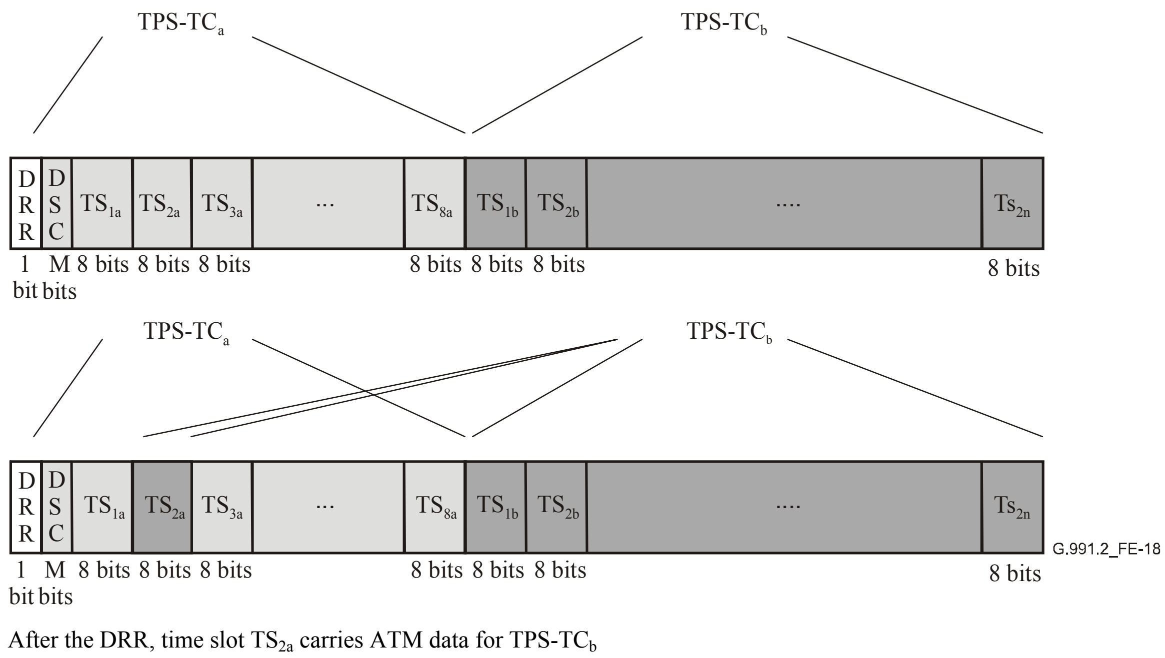


Figure E.18/G.991.2 – DRR repartitions TS_{2a} from STM bearer to ATM bearer (example)

E.10.3.10 Dual-bearer mode types for DRR

DRR is appropriate for use with some Dual-Bearer Type 1 and Type 2 TPS-TC combinations, as specified in E.10.2 and Table E.22. In particular, DRR may be used with the set of $TPS\text{-}TC_a$ and $TPS\text{-}TC_b$ combinations shown in Table E.34a.

Table E.34a/G.991.2 – TPS-TCs from dual-bearer mode Types 1 and 2 for which DRR is supported

Type	Description	$TPS\text{-}TC_a$	$TPS\text{-}TC_b$
1	STM + Broadband	Synchronous ISDN BA (E.8) LAPV5 Enveloped POTS or ISDN (E.13) STM with DSC (E.12)	Clear Channel Byte-Oriented (E.2) Aligned DS1/Fractional DS1 (E.4) Aligned D2048S/Fractional D2048S (E.7) ATM (E.9) PTM (E.11)
2	STM + Cell/Packet	Aligned DS1/Fractional DS1 (E.4) Aligned D2048S/Fractional D2048S (E.7)	ATM (E.9) PTM (E.11)
NOTE – See Table E.22 for the complete definitions of TPS-TC Types for Dual-Bearer Mode.			

E.10.3.11 Payload block ordering with DRR

The clauses describing each of the TPS-TCs define the arrangement of bits within each TPS-TC. As noted in E.10.3.4, the DRR control channel occupies 1 to 3 single-bit time slots (referred to as Z-bits). In addition, an ISDN or LAPV5 TPS-TC may use one or more Z-bits (E.8 and E.13), and a DSC (Dedicated Signalling Channel), if used, may occupy 1 to 7 Z-bits or may be mapped into the first 8-bit time slot (referred to as a B-channel). This clause defines how the different channels are mapped into the TPS-TCs.

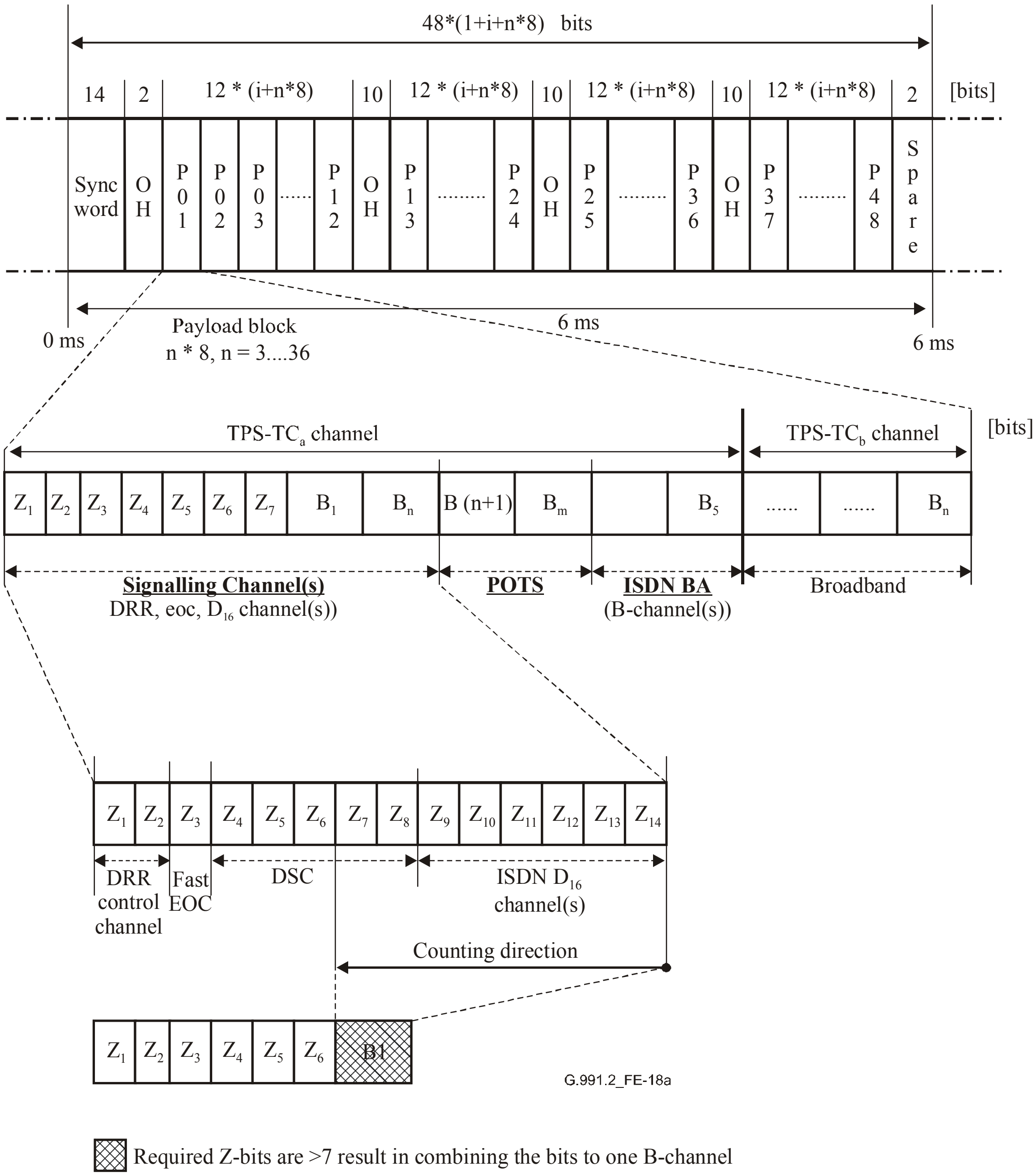


Figure E.18a/G.991.2 – SHDSL payload block ordering with DRR

Figure E.18a shows how to combine the Z-bit time slots if their number exceeds 7. The formula is based on the number of required Z-bits modulo 8.

E.11 TPS-TC for PTM transport

E.11.1 Packetized data transport

E.11.1.1 Functional model

The functional mode of packetized data transport is presented in Figure E.19. In the transmit direction, the PTM entity obtains data packets to be transported over SHDSL from the application layer interface. The PTM entity processes each packet and applies it to the γ-interface for packetized data transport. The PTM TPS-TC receives the packet from γ-interface, encapsulates it into a special frame (PTM-TC frame) and maps it into PMS-TC frame (transmission frame) for transmission over the SHDSL link.

In the receive direction, the PTM-TC frame extracted from the received PMS-TC frame is directed into the PTM-TC. The PTM-TC recovers the transported packet and delivers it to the PTM entity via the γ-interface.

The PTM path-related OAM data, including information on errored packets, shall be presented to the TPS-TC management entity providing all necessary OAM functions to support the PTM-TC.

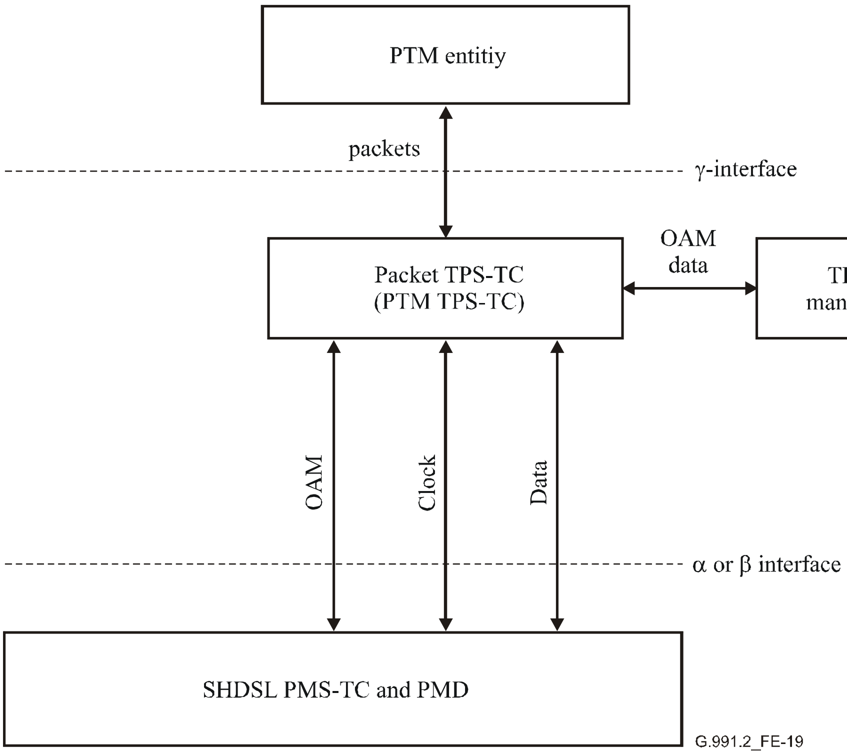


Figure E.19/G.991.2 – Functional model of PTM transport

The γ-interface is described in E.11.3.1. The α/β-interfaces are application independent and thus have the same format as for other TPS-TCs (see E.11.3.2).

E.11.2 Transport of PTM data

The bit rates of PTM data transport in the RX and TX direction on the SHDSL link are identical and may be set to any eligible value which is less than (Dual-Bearer application) or equal to the assigned maximum payload bit rate. This bit rate is set during the system configuration.

The PTM-TC shall provide full transparent data transfer between γ_{STU-C} and γ_{STU-R} interfaces (except non-correctable errors in the PMD sublayer due to the noise in the loop). The PTM-TC shall provide packet integrity over the assigned bearer channel.

E.11.3 Interface description

E.11.3.1 γ-Interface

The γ_C and γ_R reference points define the interfaces between the PTM entity and the PTM-TC at the STU-C and STU-R, respectively, as shown in Figure E.19. These interfaces are functionally identical and are independent of the contents of the transported packets. The interfaces are defined by the following flows of signals between the PTM entity and the PTM-TC sublayer:

- data flow;
- synchronization flow;
- control flow;
- OAM flow.

E.11.3.1.1 Data flow

The data flow shall consist of two contra-directional octet-based streams of packets: transmit packets (Tx_PTM) and receive packets (Rx_PTM). The packets transported in either direction over the γ-interface may be of variable length. Bits within an octet are labelled a_1 through a_8, with a_1 being the LSB and a_8 being the MSB. If either of data streams is transmitted serially, the first octet of the packet shall be transmitted first and bit a_1 of each octet shall be transmitted first as shown in Figure E.21. The Data Flow signal description is presented in Table E.35.

Table E.35/G.991.2 – PTM-TC: γ-interface data, synchronization and control flows signal summary

Flow	Signal	Description	Direction
Transmit signals			
Data	Tx_PTM	Transmit Data	PTM → PTM-TC
Control	Tx_Enbl	Asserted by PTM-TC, indicates that PTM may push packets to PTM-TC	PTM ← PTM-TC
Control	Tx_Err	Errored transmit packet (request to abort)	PTM → PTM-TC
Sync	Tx_Avbl	Asserted by the PTM entity if data is available for transmission	PTM → PTM-TC
Sync	Tx_Clk	Clock signal asserted by the PTM entity	PTM → PTM-TC
Sync	Tx_SoP	Start of the Transmit Packet	PTM → PTM-TC
Sync	Tx_EoP	End of the Transmit Packet	PTM → PTM-TC
Receive signals			
Data	Rx_PTM	Receive Data	PTM ← PTM-TC
Control	Rx_Enbl	Asserted by PTM-TC, indicates that PTM may pull packets from PTM-TC	PTM ← PTM-TC
Control	Rx_Err	Received error signals including FCS error, Invalid frame and OK	PTM ← PTM-TC
Sync	Rx_Clk	Clock Signal asserted by PTM entity	PTM → PTM-TC
Sync	Rx_SoP	Start of the Receive Packet	PTM ← PTM-TC
Sync	Rx_EoP	End of the Receive Packet	PTM ← PTM-TC

E.11.3.1.2 Synchronization flow

This flow provides synchronization between the PTM entity and the PTM-TC sublayer and contains the necessary timing to provide packet integrity during the transport. The synchronization flow shall consist of the following signals as presented in Table E.35:

- Transmit and receive timing signals (Tx_Clk, Rx_Clk), both asserted by PTM entity.
- Start of packet signals (Tx_SoP, Rx_SoP): asserted by PTM entity and by PTM-TC respectively and intended to identify the beginning of the transported packet in the corresponding direction of transmission.
- End of packet signals (Tx_EoP, Rx_EoP), asserted by PTM entity and by PTM-TC respectively and intended to identify the end of the transported packet in the corresponding direction of transmission.
- Transmit Packet Available Signal (Tx_Avbl), asserted by PTM entity to indicate that data for transmission in Tx direction is ready.

E.11.3.1.3 Control flow

Control signals are used to improve robustness of data transport between the PTM entity and the PTM-TC and are presented in Table E.35:

- Enable Signals (Tx_Enbl, Rx_Enbl): asserted by PTM-TC and indicates that data may be respectively sent from PTM entity to PTM-TC or pulled from PTM-TC to PTM entity.
- Transmit Error (Tx_Err): asserted by PTM entity and indicates that the packet or part of the packet already transported from PTM entity to PTM-TC is errored or undesirable for transmission (abort of transmitted packet).
- Receive Error (Rx_Err): asserted by PTM-TC to indicate that an errored packet is transported from PTM-TC to PTM entity.

Handling of packet errors is described in E.11.4.2.

E.11.3.1.4 OAM flow

The OAM Flow across the γ-interface exchanges OAM information between the OAM entity and its PTM related TPS-TC management functions. OAM flow is bidirectional.

The OAM flow primitives are for further study.

E.11.3.2 α/β interface

The α and β reference points define interfaces between the PTM-TC and PMS-TC at the STU-C and STU-R respectively. Both interfaces are functional, application independent, and should comply with the generic definition for all TPS-TCs as specified in clause 8.

E.11.4 PTM TPS-TC functionality

The following PTM TPS-TC functionality should be applied to both Rx and Tx direction.

E.11.4.1 Packet encapsulation

For packet encapsulation an HDLC type mechanism shall be used with detailed characteristics as specified in the following clauses.

E.11.4.1.1 Frame structure

The PTM-TC frame format shall be as shown in Figure E.20. The opening and the closing Flag Sequences shall be set to $7E_{16}$. They identify the start and the end of the frame. Only one Flag Sequence is required between two consecutive frames.

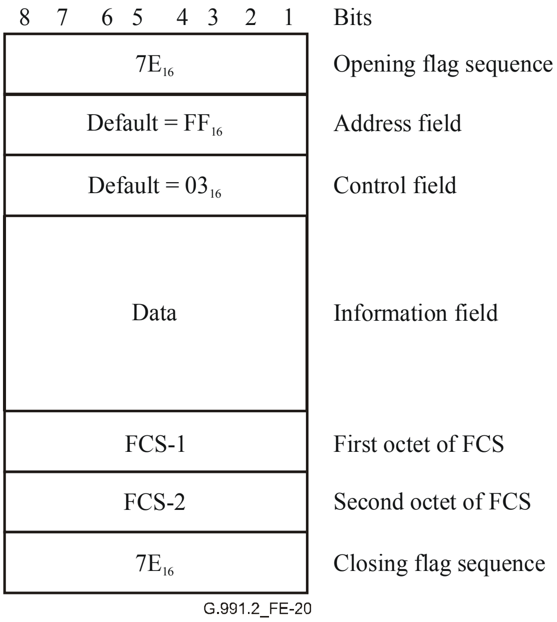


Figure E.20/G.991.2 – PTM-TC frame format

The Address and Control octets are intended for auxiliary information. They shall be set to their default values of hexadecimal FF_{16} and 03_{16} respectively if not used.

NOTE 1 – The address and Control fields may be used for different auxiliary OAM functions. The usage of these fields is for further study.

The information field shall be filled with the transported packet data. Prior to encapsulation the octets of the data shall be numbered sequentially. Octets shall be transmitted in ascending numerical order.

The frame check sequence (FCS) octets are used for packet level error monitoring, and shall be set as described in E.11.4.1.3.

After encapsulation, bits within an octet are labelled b_1 through b_8, as defined in Figure E.21. If the $\alpha(\beta)$ interface is serial by implementation, bit b_8 of each octet shall be transmitted first.

NOTE 2 – In keeping with existing labelling convention for the $\alpha(\beta)$ interface, bit b_8 (MSB) is transmitted first. The PTM-TC functionality defines a correspondence between a_1 and b_8, a_2 and b_7, etc., in order to conform to the HDLC convention of transmitting bit a_1 first.

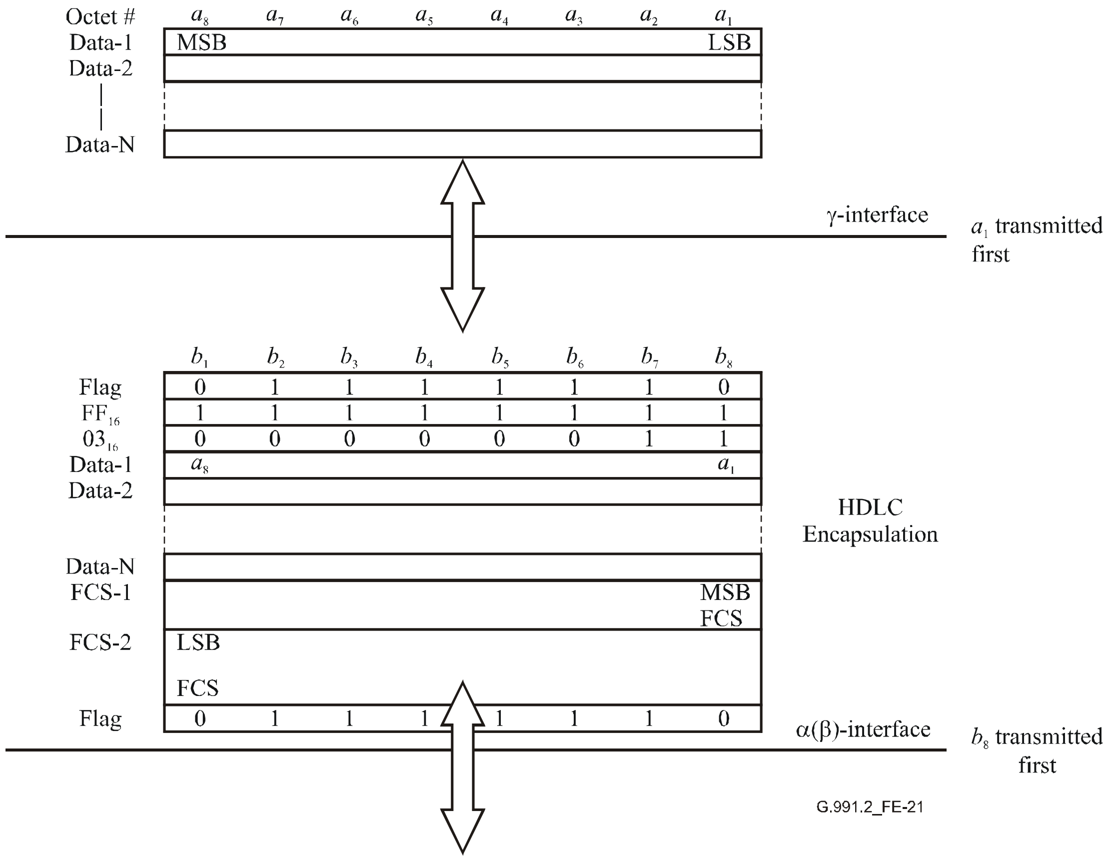


Figure E.21/G.991.2 – PTM-TC data flow

E.11.4.1.2 Octet transparency

To prevent failures due to false frame synchronization, any octet inside the PTM-TC frame that is equal to $7E_{16}$ (the Flag Sequence) or $7D_{16}$ (the Control Escape) shall be escaped as described below.

After FCS computation, the transmitter examines the entire frame between the opening and the closing Flag Sequences. Any data octets which are equal to Flag Sequence or the Control Escape shall be replaced by a two-octet sequence consisting of the Control Escape octet followed by the original octet exclusive-OR'ed with 20_{16}. In summary, the following substitutions shall be made.

- Any data octet of $7E_{16}$ – encoded as two octets $7D_{16}$, $5E_{16}$.
- Any data octet of $7D_{16}$ – encoded as two octets $7D_{16}$, $5D_{16}$.

On reception, prior to FCS computation, each Control Escape octet shall be removed and the following octet shall be exclusive OR'ed with 20_{16} (unless the following octet is $7E_{16}$ which is the flag and indicates the end of the frame, and therefore an abort has occurred). In summary, the following substitutions are made:

- any sequence of $7D_{16}$, $5E_{16}$ – replaced by the data octet $7E_{16}$.
- any sequence of $7D_{16}$, $5D_{16}$ – replaced by the data octet $7D_{16}$.
- a sequence of $7D_{16}$, $7E_{16}$ aborts the frame.

NOTE – Since octet stuffing is used, the PTM-TC frame is guaranteed to have an integer number of octets.

E.11.4.1.3 Frame check sequence

The FCS shall be calculated over all bits of the address, control, and information fields of the PTM-TC frame as defined in ISO/IEC 13239 [B13], i.e., it shall be the one's complement of the sum (modulo 2) of:

- the remainder of $x^k(x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)$ divided (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$, where k is the number of bits in the frame existing between, but not including, the last bit of the opening flag and the first bit of the FCS, excluding octets inserted for transparency (E.11.4.1.2); and
- the remainder of the division (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$, of the product of x^{16} by the content of the frame existing between, but not including, the last bit of the opening flag and the first bit of the FCS, excluding octets inserted for transparency.

The FCS is 16 bits (2 octets) in length and occupies fields FCS-1, FCS-2 of the PTM-TC frame. The FCS shall be mapped into the frame so that bit a_1 (b_8) of FCS-1 shall be the MSB of the calculated FCS, and bit a_8 (b_1) of the FCS-2 shall be the LSB of the calculated FCS (Figure E.21).

The register used to calculate the FCS at the transmitter shall be initialized to the value $FFFF_{16}$.

NOTE – As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all binary ONEs and is then modified by division by the generator polynomial, as described above, on the information field. The one's complement of the resulting remainder is transmitted as the 16-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder of the division is preset to all binary ONEs. The final remainder, after multiplication by x^{16} and then division (modulo 2) by the generator polynomial $x^{16} + x^{12} + x^5 + 1$ of the serial incoming protected bits after removal of the transparency octets and the FCS, will be 0001110100001111_2 (x^{15} through x^0, respectively) in the absence of transmission errors.

E.11.4.2 Packet error monitoring

Packet error monitoring includes detection of invalid and errored frames at receive side.

E.11.4.2.1 Invalid frames

The following conditions result in an invalid frame:

- Frames which are less than 4 octets in between flags not including transparency octets (Flag Sequence and Control Escape). These frames shall be discarded.
- Frames which contain a Control Escape octet followed immediately by a Flag (i.e., $7D_{16}$ followed by $7E_{16}$). These frames shall be passed across the γ-interface to the PTM entity.
- Frames which contain control escape sequences other than $7D_{16}$, $5E_{16}$ and $7D_{16}$, $5D_{16}$. These frames shall be passed across the γ-interface to the PTM entity.

All invalid frames shall not be counted as FCS errors. The receiver shall immediately start looking for the opening flag of a subsequent frame upon detection of an invalid frame. A corresponding receive error message (Rx_Err – E.11.3.1.3) shall be sent across the γ-interface to the PTM entity.

E.11.4.2.2 Errored frames

A received frame shall be qualified as an errored frame (FCS-errored) if the CRC calculation result for this frame is different from the one described in E.11.4.1.3. Errored frames shall be passed across the γ-Interface. A corresponding receive error message (Rx_Err – E.11.3.1.3) shall be sent across the γ-interface to the PTM entity.

E.11.4.3 Data rate decoupling

Data rate decoupling is accomplished by filling the time gaps between transmitted PTM-TC frames with additional Flag Sequences ($7E_{16}$). Additional Flag Sequences shall be inserted at the transmit side between the closing Flag Sequence of the last transmitted PTM-TC frame and the subsequent opening Flag Sequence of the next PTM-TC frame, and discarded at the receive side respectively.

E.11.4.4 Frame delineation

The PTM-TC frames should be delineated by detecting of Flag Sequence. The incoming stream is examined on an octet-by-octet basis for the value $7E_{16}$. Two (or more) consecutive flag sequences constitute an empty frame (frames), which shall be discarded, and not counted as a FCS error.

E.11.4.5 Mapping to the SHDSL framing

The PMS-TC provides a clear channel to the PTM-TC and packets are mapped into the SHDSL payload on a byte-by-byte basis. At the STU-C, packets are mapped across the logical α interface while at the STU-R, packets cross the logical β interface. At the alpha and beta interface, logical data and clock lines are present. Packet alignment to the SHDSL frame is optional. The provided bandwidth by the PMS-TC is $k_s = i + n \times 8$ with $0 \le i < 7$ and $3 \le n \le 36$. For n = 36, *i* is restricted to values of 0 and 1. Note that optional extensions described in Annex F allow values of *n* up to 89.

In the optional *M*-pair mode, PTM data is carried over all pairs using interleaving, as described in 8.2. In *M*-pair mode only multiples of *M* time slots may be supported. Each Payload Sub-Block is treated as containing $M \times n$ 8-bit time slots. Each byte from the input PTM data stream is mapped MSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, … , time slot *n*. A total of $M \times k_s$ bits (or $M \times n$ bytes) of contiguous data shall be contained within each Sub-Block, as specified in 8.1, where $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Note that optional extensions described in Annex F allow values of *n* up to 89. The bytes from the input PTM data stream shall be interleaved among all *M* pairs, such, where byte b_k is carried on Pair 1, byte b_{k+1} is carried in the corresponding time slot on Pair 2, etc. Byte b_{k+M-1} is carried in the corresponding time slot on Pair *M*.

E.12 TPS-TC for STM with a Dedicated Signalling Channel (DSC)

In certain STM applications, including some channelized voice and data applications, a dedicated channel is desired to carry higher-layer telephony signalling for the STM time slots (e.g., per Telcordia GR-303 [B14] or ETSI V5 [9] and [B16]). This TPS-TC defines a transport format for channelized STM with a Dedicated Signalling Channel (DSC).

Figure E.22 shows the alignment of STM time slots and the DSC within the SHDSL frame. Each Payload Sub-Block contains a DSC (*i* bits in length, where $1 \le i \le 7$), followed by *n* 8-bit time slots referred to as TS_1 ... TS_n. Note that the details of the protocols used over the DSC are beyond the scope of this Recommendation.

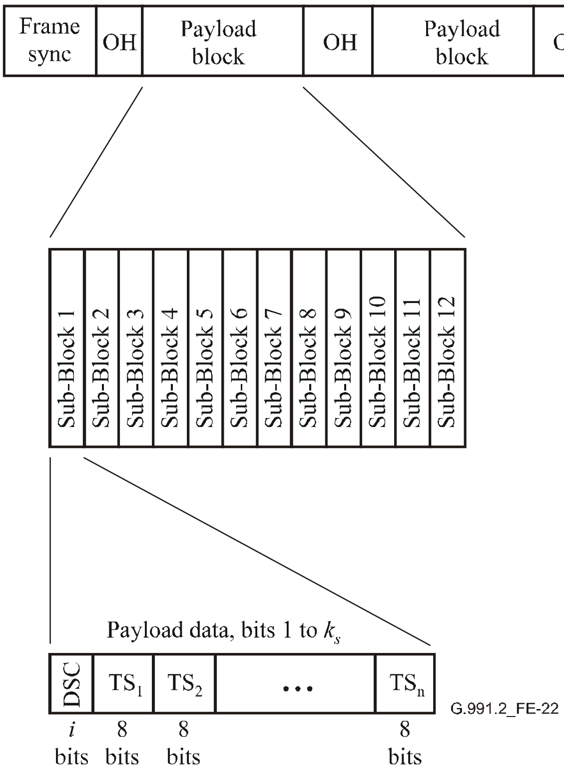


Figure E.22/G.991.2 – STM framing with a dedicated signalling channel

In the optional *M*-pair mode, both the STM and the DSC are carried over all *M* pairs using interleaving, as described in 8.2. A total of $M \times n$ time slots shall be transported per SHDSL Payload Sub-Block. The STM time slots shall be interleaved among all *M* wire pairs, such that pair *m* carries the *m*th time slot out of every block of *M* time slots. The DSC is interleaved among the *M* pairs such that it occupies the first *i* bit positions within each Payload Sub-Block on each of the *M* wire pairs. *i* may take any value in the range $1 \leq i \leq 7$, so a total of $M \times i$ bits make up the DSC. *i* bits of contiguous DSC data shall be contained within a Sub-Block on Pair 1, and the following sets of *i* bits of contiguous DSC data shall be contained within the corresponding Sub-Blocks of subsequent pairs. See Figure E.23 for additional details.

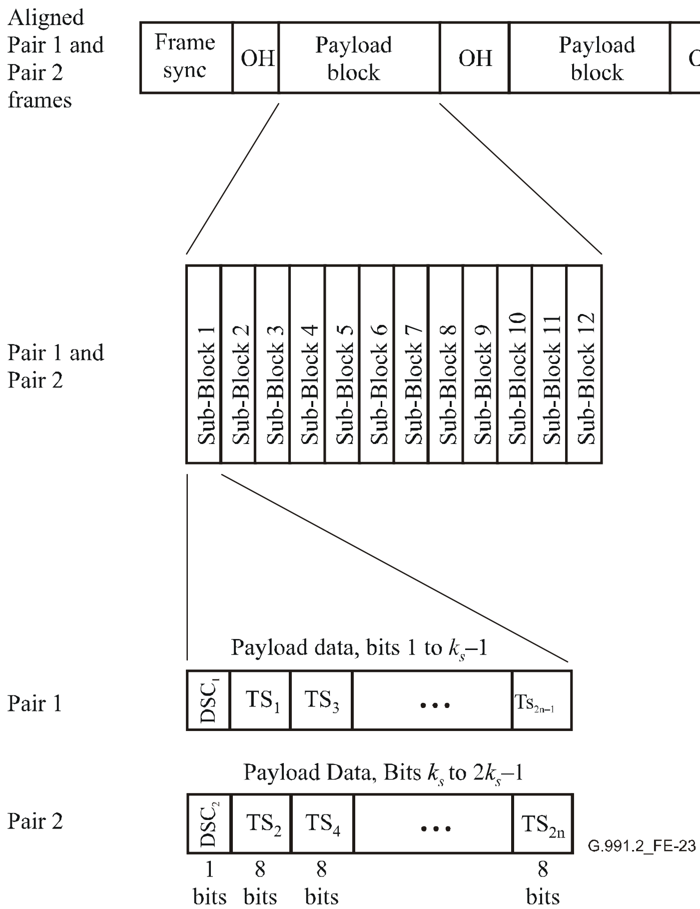


Figure E.23/G.991.2 – *M*-pair STM framing with a dedicated signalling channel (for the case where *M* = 2 and *i* = 1)

E.13 TPS-TC for LAPV5 enveloped POTS or ISDN

The mapping and time slot allocation of STM based, LAPV5 controlled, PSTN and ISDN-BA transport is specified, which is for ISDN an alternative procedure to the simple use of D-channel messages as described in E.8. It is not expected that the TPS-TC described in this clause will be used simultaneously with the ISDN transport described in E.8 or the POTS transport described in E.13.

This clause describes the transport of POTS and ISDN over a combination of the SHDSL EOC, Z-channels, and B-channels. Control and signalling information is transported over either the EOC, Z, or first B-channels using frame-based V5 wrappings. The POTS voice and ISDN B-channels are transported over STM based pre-assigned SHDSL B-channels.

E.13.1 Signalling channel

Signalling as well as the other POTS or ISDN related messages are transported over a common signalling channel. Depending on the required amount of signalling and port control information, either a portion of the SHDSL EOC or a portion of the payload sub-block may be used for this signalling transport. If the SHDSL EOC is used for the signalling transport, then the V5 signalling messages are wrapped using SHDSL EOC Message IDs. If the SHDSL EOC is not used for this transport, then within the SHDSL frame, the signalling bits are either mapped into 1 to 7 Z-channel(s), or are mapped into the first B-channel time slot of each sub-block.

In order to transport signalling information, the STU-C and STU-R must agree on the particular signalling channel to be used. The signalling channel is identified using parameter (N_{sig}) with a range of 0 to 8 plus the value 16. The value 0 indicates that the signalling is on the SHDSL EOC. The values 1 through 7 indicate that there are 1 through 7 Z-channel bits present and that the signalling is to be transported there. A value of 8/16 indicates that the signalling is transported in the first one/two B-channel time slots of each sub-block. Other values of N_{sig}, such as 24 and 32, are for future study.

E.13.2 Mapping of 64 kbit/s payload channels

One or multiple 64 kbit/s POTS voice channels and/or one or multiple ISDN B-channel pairs are mapped onto B-channels in the SHDSL sub-frame. The POTS channels are mapped sequentially into the first B-channels of each sub-frame after any signalling B-channels. The ISDN B-channel pairs are mapped into the first B-channels of each sub-frame after any signalling or POTS B-channels. These mappings are similar to those in E.8 and E.12.

In order to transport payload information, both the STU-C and STU-R have to agree as to how many POTS and ISDN BA circuits to allocate B-channels for. The number of channels shall be the same for both directions. The number of POTS circuits shall be specified as an integer (N_{pots}) with a range of 0 to 35. The number of ISDN circuits shall be specified as an integer (N_{isdn}) with a range of 0 to 17. (Other values are for future study.)

The total number of B-channels consumed for the control and payload transport is (1 or 2 if N_{sig} = 8 or 16, else 0) + N_{pots} + (2 × N_{isdn}). The remaining B-channels are available for the underlying application.

E.13.3 Signalling and port control

In the case where the common signalling channel is carried over the SHDSL EOC, (that is N_{sig} = 0), the TPS-TC is addressed by the ISDN Message IDs within the EOC (IDs 20 and 148, see 9.5.5.6). Octet 2 is not used and octets 3 through *n* contain the LAPV5 message. The message content is enveloped by LAPV5-EF. Envelope functions and message contents are specified in ETSI EN 300 324-1 [9] and ETSI EG 201 900-1 [10]. See Tables E.36 and E.37 for details.

Table E.36/G.991.2 – ISDN Request – Message ID 20

Octet #	Contents	Data type	Reference
1	20	Message ID	
2	Not used		
3 to *n*	LAPV5 message code		

Table E.37/G.991.2 – ISDN Response – Message ID 148

Octet #	Contents	Data type	Reference
1	148	Message ID	
2	Not used		
3 to *n*	LAPV5 message code		

In ETSI EN 300 324-1 [9] clause 9.1.5, the maximum frame size is specified as 533 octets. In the SHDSL EOC, the limit is 75 octets. Applications which require control and signalling frames larger than 76 octets should choose N_{sig} > 0.

In the case where the common signalling channel is carried over the Z- or B-channel, (that is $N_{sig} > 0$), the message format is as specified in ETSI EN 300 324-1 [9], clause 9. This mode shall use all of clause 9, including subclauses for the flag sequence, interframe fill time, transparency, frame check sequence, format conversion, and invalid frames which are not used in the EOC mode above.

E.13.4 Protocol architecture for LAPV5 enveloped POTS and ISDN

Table E.38 shows the layered structure for LAPV5 enveloped POTS and ISDN services. Note that the left lower column is for EOC signalling transport and the right lower column is for Z- or B-channel signalling transport.

Table E.38/G.991.2 – Protocol architecture

<table>
<tr><td>POTS signalling
ETSI EN 300 324-1 [9], clause 13</td><td colspan="2">POTS/ISDN port control
ETSI EN 300 324-1 [9], clause 14</td><td>ISDN signalling</td></tr>
<tr><td colspan="3">LAPV5-DL
ETSI EN 300 324-1 [9], clause 10</td><td>LAPD</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td colspan="2">LAPV5-EF address
ETSI EN 300 324-1 [9], clause 9.1.4</td><td colspan="2">LAPV5-EF
ETSI EN 300 324-1 [9], clause 9</td></tr>
<tr><td colspan="2">TPS-TC
Message ID: LAPV5 enveloped POTS and ISDN</td><td colspan="2">Signalling Z- or B-channels</td></tr>
<tr><td colspan="4">PMD-TC, PMS-TC</td></tr>
<tr><td colspan="4">NOTE – The ISDN signalling (LAPD and layer 3) is part of the ISDN-TE functionality and outside the scope of this Recommendation.</td></tr>
</table>

The LAPV5-EF envelope address (ETSI EN 300 324-1 [9], clause 9) envelopes the frames for signalling of an individual ISDN access, or for POTS signalling or for POTS/ISDN port control.

For the reliable transport of POTS signalling and POTS/ISDN port control messages, the data link protocol LAPV5-DL is used which is a simplified version of LAPD. The LAPV5-DL protocol is specified as in ETSI EN 300 324-1 [9], clause 10.

As in ETSI EG 201 900-1 [10] (Loop Emulation Service using AAL2), the following differences with respect to ETSI EN 300 324-1 [9] exist:

- Only one common instance of LAPV5-DL is used for both the POTS signalling and the POTS/ISDN port control.
- The LAPV5-DL address takes the value of all zeros.
- POTS signalling messages and POTS/ISDN port control messages are distinguished by means of the Message type information element.
- A common error handling procedure for "unrecognized message type" errors is used for both the PSTN and Control protocol: Whenever an unrecognized message is received, the protocol entity shall generate an internal error indication and ignore the message.
- ISDN signalling is conveyed via frame relay as described in ETSI EN 300 324-1 [9], clause 11. This means that the customer's D-channel data link layer protocol is not fully terminated.

NOTE – The existing TPS-TC for ISDN as described in E.8 remains unchanged. It provides a lean alternative for networks where no POTS, but only ISDN is provided.

E.13.5 System procedures

E.13.5.1 System start-up

With regard to the remainder of this subclause, actions required for any items that are not provisioned shall be ignored.

NOTE – The procedures are derived from 5.4.4.1 and 5.4.4.2 of af-vmoa-0145.000 [B15].

E.13.5.1.1 Preconditions

The initial states of the various Finite State Machines (FSM) involved in the start-up are as follows:

Table E.39/G.991.2 – Initial states of finite state machines

FSM	Initial state
Port Control Protocol FSM	Out of Service (AN0/LE0)
PSTN Port Status FSM	Blocked (AN1.0/LE1.0)
ISDN BA Port Status FSM	Blocked (AN1.0/LE1.0)
PSTN Protocol FSM	Port Blocked (AN6/LE6)
NOTE – These FSMs are defined in the V5 specifications ETSI EN 300 324-1 [9]. The "LE" states relate to the STU-C side and the "AN" states relate to the STU-R side of the connection.	

E.13.5.1.2 Normal procedure

a) Activation of LAPV5-DL: MDL-Establish-Request shall be sent to the LAPV5-DL.

b) When MDL-ESTABLISH-CONFIRM or MDL-ESTABLISH-INDICATION is received from the LAPV5-DL, START-TRAFFIC shall be sent to the port control protocol FSMs.

c) Entering the normal state.

d) Post-processing: The STU-C side shall initiate the coordinated unblock procedure for all relevant user ports. The STU-R side shall not initiate unblocking at this time.

E.13.5.1.3 Exceptional procedures in case of failure in system start-up

When the system start-up cannot be continued for some reason (e.g., LAPV5-DL failure) and is unable to enter the normal state, system restart shall be performed.

E.13.5.2 System restart

System restart refers to the re-starting of a single LAPV5-DL protocol instance between a STU-C side and a STU-R side. Under system restart the following actions apply:

1) The interface shall be brought into a state in which no established LAPV5-DL exists.

NOTE 1 – The remote side takes this as a trigger for system restart.

2) Timer TL1 shall be started.

3) On expiry of TL1 system start-up shall be performed.

Timer TL1 shall have a predefined value of 20 seconds.

NOTE 2 – Timer TL1 triggers system start-up. It is needed to guarantee that the release of the LAPV5-DL is recognized at the remote side and hence both the STU-R side and STU-C side undergo system start-up. This timer is started when the system has been stopped for any reason during the system start-up or normal operation. It shall also be run prior to invoking the system start-up when performing a cold start.

Situations where system restart shall be applied:

a) Reception of Release-Indication of LAPV5-DL.

b) Under request by the Management System.

E.13.6 N_{sig}, N_{pots} and N_{isdn}

In order to support interoperability, the STU-C and STU-R need to agree on the values of the parameters N_{sig}, N_{pots} and N_{isdn}. This agreement may be by prior agreement outside the scope of this annex.

Alternatively, the STU-C may configure the STU-R via the SHDSL EOC. To support this, there is a Message ID for LAPV5 POTS and ISDN Set-up. The purpose is to specify the values for N_{sig}, N_{pots} and N_{isdn}. The Message ID 21 is the Request from the STU-C to the STU-R and Message ID 149 is the Response from the STU-R to the STU-C. See Tables E.40 and E.41 for details.

The request message allows the STU-C to configure the STU-R with the values of N_{sig}, N_{pots} and N_{isdn}. The response message is an acknowledge from the STU-R to STU-C. If octets 2, 3, and 4 of the response match those in the request, then the response indicates that the STU-R accepts the values sent by the STU-C. If the STU-R does not accept the values proposed by the STU-C, it may respond with the octets 2, 3, and/or 4 modified to contain an acceptable value and also the MSB of each octet in question set. The STU-R should respond to a request within 500 ms. In the event that the STU-R does not respond, the STU-C will try at least three times before concluding that the option cannot be supported.

Table E.40/G.991.2 – LAPV5 POTS and ISDN Set-up Request – Message ID 21

Octet #	Contents	Data type	Note
1	21	Message ID	
2	N_{sig}	Unsigned char	
3	N_{pots}	Unsigned char	
4	N_{isdn}	Unsigned char	

Table E.41/G.991.2 – LAPV5 POTS and ISDN Set-up Response – Message ID 149

Octet #	Contents	Data type	Note
1	149	Message ID	
2	N_{sig}	Unsigned char	
3	N_{pots}	Unsigned char	
4	N_{isdn}	Unsigned char	

Annex F

Region 1 requirements for payload data rates up to 5696 kbit/s

F.1 Scope

The clauses in this annex provide the additions and modifications to the corresponding clauses in the main body and Annex A for payload data rates up to 5696 kbit/s. Support for this annex is optional.

NOTE – Some countries have standards for spectrum management requirements that limit the length of the lines for transmission of certain signal levels in this annex, for example Spectrum Management Standard T1.417 applies in the United States access network.

F.2 Data rate

The operation of the STU in data mode at the specified information rate shall be as specified in Table F.1.

Table F.1/G.991.2 – Framed data mode rates

Payload data rate, *R* (kbit/s)	Modulation	Symbol rate (ksymbol/s)	*K* (Bits per symbol)
$R = n \times 64 + (i) \times 8$	16-TCPAM	$(R + 8) \div 3$	3
$R = n \times 64 + (i) \times 8$	32-TCPAM	$(R + 8) \div 4$	4

As specified in the main body (per clause 5, reiterated in 7.1.1, 8.1 and 8.2), the allowed single-pair rates are given by $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. In these clauses, the allowed values i are further restricted to 0 or 1 for $n = 36$. These definitions correspond to (payload) data rates from 192 kbit/s to 2.312 Mbit/s in increments of 8 kbit/s.

This annex extends those rates. It is applicable for single-pair rates given by $n \times 64 + i \times 8$ kbit/s. For 16-TCPAM, $36 \le n \le 60$ and $0 \le i \le 7$. For 16-TCPAM and n = 36, the applicable values of i are $2 \le i \le 7$. For 16-TCPAM and $n = 60$, the applicable value of i is 0. This corresponds to (payload) data rates from 2320 kbit/s to 3840 kbit/s in increments of 8 kbit/s for 16-TCPAM. For 32-TCPAM, $12 \le n \le 89$ and $0 \le i \le 7$. For 32-TCPAM and $n = 89$, the applicable value of i is 0. This corresponds to (payload) data rates from 768 kbit/s to 5696 kbit/s in increments of 8 kbit/s for 32-TCPAM.

This annex is also applicable for optional operation on more than one pair (*M*-pair mode).

F.2.1 Support for multiple encodings

Support for the data rates specified in this annex is optional, and, as such, an STU supporting this annex is not required to support all specified data rates. For each rate that an STU-R supports, it shall support all available encodings (i.e., both 16- and 32-TCPAM for rates where both encodings are specified). Support for multiple encodings is optional at the STU-C.

F.2.2 G.994.1 Pre-activation sequence

As specified in 6.4, ITU-T Rec. G.994.1 is used to begin the pre-activation sequence.

To support a wide range of data rates and multiple encodings, this clause introduces a new way to encode data rates in G.994.1 code points. This method of encoding rates is used for both the PMMS rates and the training rates. Data rates are encoded as a set of ranges, where each range is expressed as a 3-tuple (minimum, maximum, step). The 3-tuple represents all rates of the form $(m + k \times s) \times (64\ \text{kbit/s})$ where m is the minimum value, s is the step value, and k is the set of all integers greater than or equal to zero such that $m + k \times s$ is less than or equal to the maximum value. Thus, for example, the 3-tuple (40, 70, 10) represents the rates 40×64 kbit/s, 50×64 kbit/s, 60×64 kbit/s, and 70×64 kbit/s.

Each data rate parameter in this annex can be expressed as a set of between 1 to 8 ranges, where the supported rates are the union of those supported by the individual ranges. Thus, for example, the 3-tuples (20, 30, 4), (40, 70, 10) represent the rates 20×64 kbit/s, 24×64 kbit/s, 28×64 kbit/s, 40×64 kbit/s, 50×64 kbit/s, 60×64 kbit/s, and 70×64 kbit/s. If all bits of the extended base data rate minimum and maximum are set to zero, then those rates are not supported for line probe. If only one range of rates is required, then only the octets associated with (min1, max1, step1) shall be sent.

Also, in many cases, the values in the data range 3-tuple can be less than or equal to 89 (representing the maximum payload data rate of 5696 supported in this annex). When using G.994.1 code point representation, only 6 bits are available for the value of an NPar(3). To support numbers greater than 63, the value must be split across multiple octets. When encoding a data range using G.994.1, 4 octets are used, where the first octet contains the highest order bit from each of the values in the 3-tuple. This is illustrated in Table 11.16.10/G.994.1.

The complete set of rate capabilities shall be the union of the extended rates specified in Annex F (G.994.1 Table 11.16.0.1 bits 4-6 and Table 11.16.0.2 bits 1-3) with the non-extended rates specified in Annex A (G.994.1 Table 11.16 bits 1-4).

Ranges of rates may overlap and may contain some rates which are identical. For example, the 3-tuples (40, 60, 10) and (50, 70, 5) would be a valid set of ranges. In this case, the union of these two 3-tuples would be the rates 40×64 kbit/s, 50×64 kbit/s, 55×64 kbit/s, 60×64 kbit/s, 65×64 kbit/s, and 70×64 kbit/s. Note that, for PMMS, if two ranges contain some rates which are identical, the probe waveforms associated with these identical rates are only sent once.

The following definition is added to the G.994.1 code point definitions in 6.4.1 for the support of the extended data rates specified in this annex.

Extended Base Data Rate: These octets are used to specify payload rates for this annex, as follows:

– The PMMS octets indicate rates for line probing segments. Note that while PMMS uses 2-PAM modulation, the PMMS symbol rates are specified assuming 32 TCPAM encoding, so the PMMS symbol rate (in ksymbol/s) would be equal to the (payload data rate (kbit/s) + 8 kbit/s)/4. If both symmetric and asymmetric PSDs are indicated, then all of the indicated symmetric PSDs shall be sent first, followed by all of the indicated asymmetric PSDs. Valid values for min and max shall be between 49 and 89, inclusive, and valid values for step shall be between 1 and 40, inclusive. The variables j5 and j6 associated with the PMMS rates shall be independent, and shall range from 1 to 8, inclusive. If only one range of rates is required, then only the octets associated with (min1, max1, step1) shall be sent.
– The training parameter octets indicate extended payload data rates supported.
– In CLR, upstream training parameters indicate which data mode rates the STU-R is capable of transmitting and downstream training parameters indicate which data mode rates the STU-R is capable of receiving. If the optional line probe is used, the receiver training parameters will be further limited by the probe results. Valid values for minimum and maximum shall be between 36 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM. Valid values for step shall be between 1 and 89, inclusive. The variables j1, j2, j3 and j4 associated with the training rates shall be independent, and shall range from 1 to 8, inclusive. The STU-R shall indicate support for both 16- and 32-TCPAM for all supported rates for which both encodings are defined in this annex.

– In CL, downstream training parameters indicate which data mode rates the STU-C is capable of transmitting and upstream training parameters indicate which data mode rates the STU-C is capable of receiving. Valid values for minimum and maximum shall be between 36 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM. Valid values for step shall be between 1 and 89, inclusive. The variables j1, j2, j3 and j4 associated with the training rates shall be independent, and shall range from 1 to 8, inclusive. If optional line probe is used, the receiver training parameters will be further limited by the probe results.

– Data rate selections shall be specified in MP and MS messages by setting the maximum and minimum rates to the same value.

F.3 Mapper

The $K + 1$ bits $Y_K(m), \ldots, Y_1(m)$, and $Y_0(m)$ shall be mapped to a level $x(m)$. In 6.1.2.3, the mapper function is specified for 16-TCPAM. This annex extends that mapping to include both 16- and 32-TCPAM encodings. Table F.2 shows the bit to level mapping for 16- and 32-level mapping.

Table F.2/G.991.2 – Mapping of bits to PAM levels

Y_4(m)	Y_3(m)	Y_2(m)	Y_1(m)	Y_0(m)	32-PAM (5 bits)	16-PAM (4 bits)
0	0	0	0	0	–31/32	–15/16
0	0	0	0	1	–29/32	–13/16
0	0	0	1	0	–27/32	–11/16
0	0	0	1	1	–25/32	–9/16
0	0	1	0	0	–23/32	–7/16
0	0	1	0	1	–21/32	–5/16
0	0	1	1	0	–19/32	–3/16
0	0	1	1	1	–17/32	–1/16
0	1	1	0	0	–15/32	1/16
0	1	1	0	1	–13/32	3/16
0	1	1	1	0	–11/32	5/16
0	1	1	1	1	–9/32	7/16
0	1	0	0	0	–7/32	9/16
0	1	0	0	1	–5/32	11/16
0	1	0	1	0	–3/32	13/16
0	1	0	1	1	–1/32	15/16
1	1	0	0	0	1/32	–
1	1	0	0	1	3/32	–
1	1	0	1	0	5/32	–
1	1	0	1	1	7/32	–
1	1	1	0	0	9/32	–
1	1	1	0	1	11/32	–
1	1	1	1	0	13/32	–
1	1	1	1	1	15/32	–
1	0	1	0	0	17/32	–
1	0	1	0	1	19/32	–

Table F.2/G.991.2 – Mapping of bits to PAM levels

Y_4(m)	Y_3(m)	Y_2(m)	Y_1(m)	Y_0(m)	32-PAM (5 bits)	16-PAM (4 bits)
1	0	1	1	0	21/32	–
1	0	1	1	1	23/32	–
1	0	0	0	0	25/32	–
1	0	0	0	1	27/32	–
1	0	0	1	0	29/32	–
1	0	0	1	1	31/32	–

F.4 PSD masks

For symmetric PSDs using 16-TCPAM payload data rates greater than or equal to 2320 kbit/s, and for symmetric PSDs using 32-TCPAM payload data rates greater than or equal to 768 kbit/s, the measured transmit PSD of each STU shall not exceed the PSD masks specified in this clause ($PSDMASK_{\text{SHDSL}}(f)$), and the measured total power into 135 Ω shall fall within the range specified in this clause ($P_{SHDSL} \pm 0.5$ dB).

The inband PSD for $0 < f < 2.0$ MHz shall be measured with a 10 kHz resolution bandwidth.

NOTE 1 – Large PSD variations over narrow frequency intervals (for example near the junction of the main lobe with the noise floor) might require a smaller resolution bandwidth (RBW) to be used. A good rule of thumb is to choose RBW such that there is no more than 1 dB change in the signal PSD across the RBW.

For all values of framed data rate available in the STU, the following set of PSD masks ($PSDMASK_{\text{SHDSL}}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) =$$

$$\begin{cases} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_{sym}} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\dfrac{\pi f}{N f_{sym}}\right)^2} \times \dfrac{1}{1+\left(\dfrac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}} \text{ W/Hz}, & f < f_{\text{int}} \\ -90 \text{ dBm/Hz peak, with max power in the } [f, f+1 \text{ MHz}] \text{ window of} & \\ [10\log_{10}(0.5683\times 10^{-4} \times f^{-1.5}) + 90] \text{ dBm}, & f_{\text{int}} \le f \le 3.184 \text{ MHz} \\ -90 \text{ dBm/Hz peak, with max power in the } [f, f+1 \text{ MHz}] \text{ window of} & \\ -50 \text{ dBm}, & 3.184 \text{ MHz} \le f \le 12 \text{ MHz} \end{cases}$$

where *MaskOffsetdB(f)* is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1 + 0.4 \times \dfrac{f_{3dB} - f}{f_{3dB}}, & f < f_{3dB} \\ 1 \text{ dB}, & f \ge f_{3dB} \end{cases}$$

f_{int} is the frequency where the two functions governing $PSDMASK_{SHDSL}(f)$ intersect in the range 0 to f_{sym}. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, *N*, f_{sym}, f_{3dB}, and P_{SHDSL} are defined in Table F.3. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload bit rate. The variables f, f_{sym}, f_{int}, and f_{3dB} in the equations are in units of Hz.

Table F.3/G.991.2 (Part 1) – Symmetric PSD parameters, 16-TCPAM

Payload bit rate, *R* (kbit/s)	K_{SHDSL}	*Order*	*N*	f_{sym} (ksymbol/s)	f_{3dB}	P_{SHDSL} (dBm)
2320 ≤ R ≤ 3840	7.86	6	1	(*R* + 8)/3	1.0 × f_{sym}/2	13.5

Table F.3/G.991.2 (Part 2) – Symmetric PSD parameters, 32-TCPAM

Payload bit rate, *R* (kbit/s)	K_{SHDSL}	*Order*	*N*	f_{sym} (ksymbol/s)	f_{3dB}	P_{SHDSL} (dBm)
768 ≤ R ≤ 5696	7.86	6	1	(*R* + 8)/4	1.0 × f_{sym}/2	13.5

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range P_{SHDSL} ± 0.5 dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range P_{SHDSL} ± 0.5 dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure F.1 shows the PSD masks with 0 dB power backoff for payload data rates of 3840 (16-TCPAM) and 5696 (32-TCPAM) kbit/s.

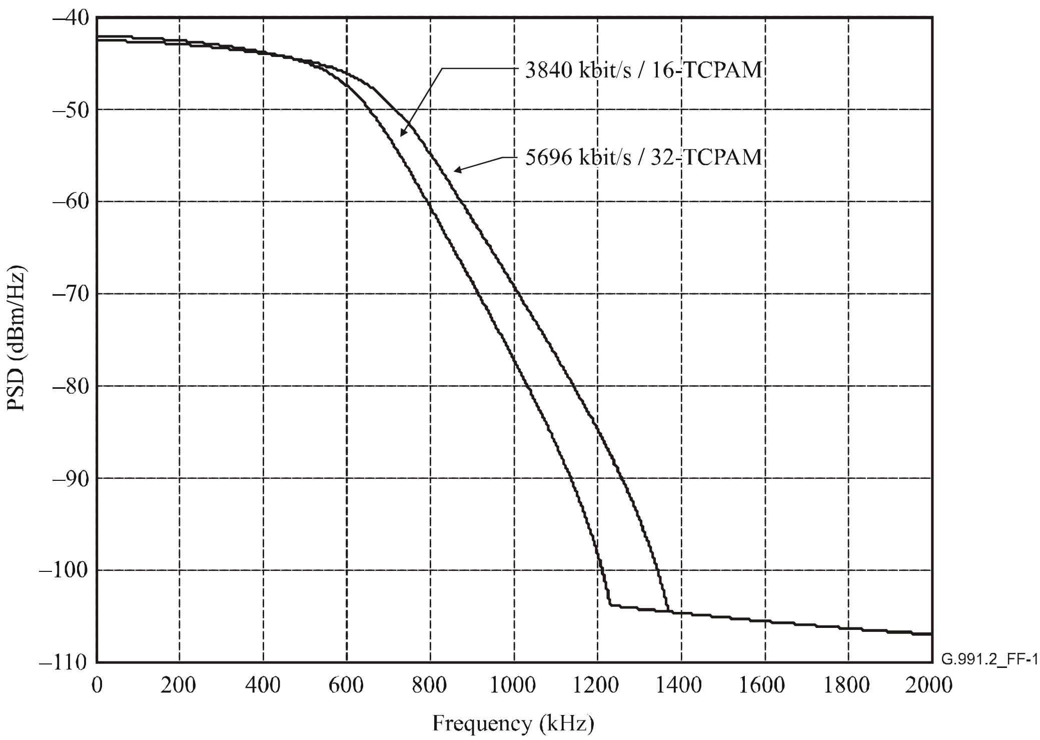


Figure F.1/G.991.2 – PSD masks for 0 dB power backoff

The equation for the nominal PSD measured at the terminals is:

$$\text{Nominal}PSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \dfrac{K_{SHDSL}}{135} \times \dfrac{1}{f_{sym}} \times \dfrac{\left[\sin\left(\dfrac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\dfrac{\pi f}{N f_{sym}}\right)^2} \times \dfrac{1}{1+\left(\dfrac{f}{f_{3dB}}\right)^{2\times Order}} \times \dfrac{f^2}{f^2+f_c^2} \text{ W/Hz}, & f < f_{int} \\ 0.5683\times 10^{-4} \times f^{-1.5} \text{ W/Hz}, & f_{int} \le f \le 3.184 \text{ MHz} \\ -100 \text{ dBm/Hz}, & 3.184 \text{ MHz} \le f \le 12 \text{ MHz} \end{cases}$$

where f_c is the transformer cut-off frequency, assumed to be 5 kHz. The variables f, f_{sym}, f_{int}, and f_{3dB} in the equations are in units of Hz. Figure F.2 shows the nominal transmit PSDs with 13.5 dBm power for payload data rates of 3840 (16-TCPAM) and 5696 (32-TCPAM) kbit/s.

NOTE 2 – The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations as representative of typical implementations.

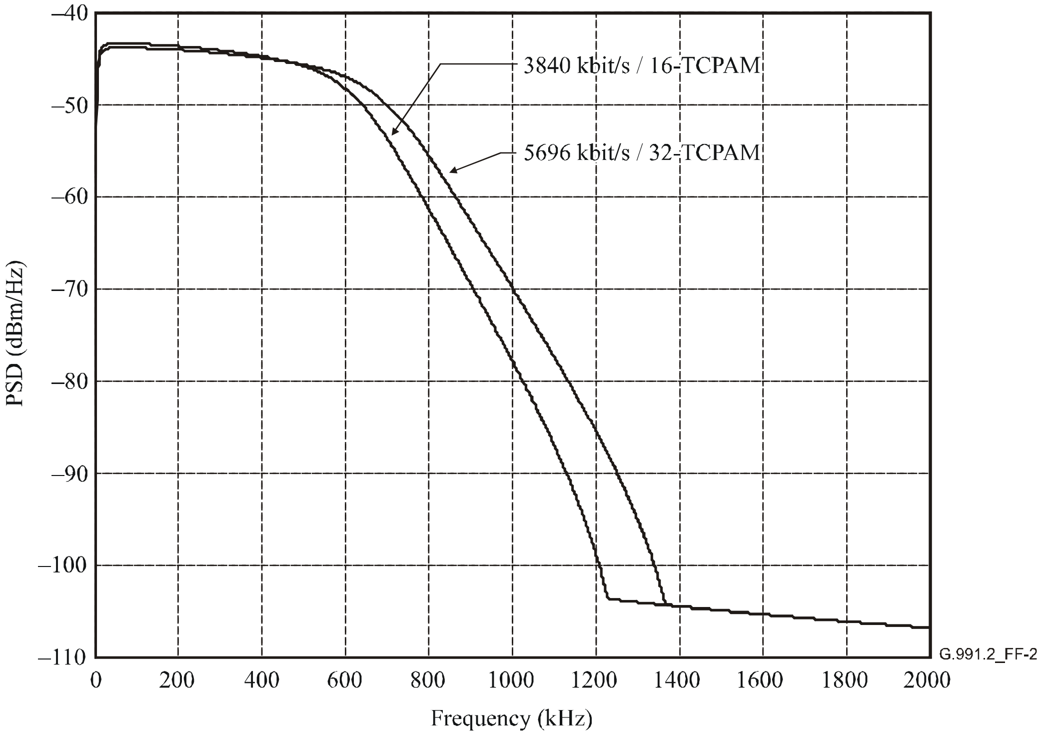


Figure F.2/G.991.2 – Nominal PSDs for 0 dB power backoff

F.5 Crosstalk interference requirements

Table F.4 shows the minimum set of test loops and crosstalk combinations required for testing SHDSL margins. A compliant unit shall pass the BER test described in A.3.1 for all crosstalk scenarios and test loops defined in Table F.4 for all supported data rates and modulation type (e.g., 16-TCPAM or 32-TCPAM). 0 dB Power Backoff shall be used for both the STU-C and STU-R. The calibration procedure and testing methods used shall be identical to those used for Annex A. The test loops and disturbers are identical to the corresponding cases in Annex A.

Table F.4/G.991.2 – Crosstalk scenarios and required SHDSL noise margins (Note)

Test	Test loop (from Figure A.1)	L (× 1000')	Test unit	Payload data rate (kbit/s)	Modulation	PSD	Interferer combination	Required margin (dB)
1	S	4.5	STU-C	3840	16-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 4)	5 + Δ*
2	S	4.5	STU-R	3840	16-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 14)	5 + Δ*
3	S	4.9	STU-C	3392	16-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 4)	5 + Δ*
4	S	4.9	STU-R	3392	16-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 14)	5 + Δ*
5	S	5.7	STU-C	2560	16-TCPAM	Symmetric	49 SHDSL sym 2304	5 + Δ*

Table F.4/G.991.2 – Crosstalk scenarios and required SHDSL noise margins (Note)

Test	Test loop (from Figure A.1)	L (× 1000')	Test unit	Payload data rate (kbit/s)	Modulation	PSD	Interferer combination	Required margin (dB)
							(Case 11)	
6	S	5.7	STU-R	2560	16-TCPAM	Symmetric	49 SHDSL sym 2304 (Case 11)	5 + Δ*
7	S	2.8	STU-C	5696	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 4)	5 + Δ*
8	S	2.8	STU-R	5696	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 14)	5 + Δ*
9	S	3.1	STU-C	5056	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 4)	5 + Δ*
10	S	3.1	STU-R	5056	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 14)	5 + Δ*
11	S	4.2	STU-C	3392	32-TCPAM	Symmetric	49 SHDSL sym 2304 (Case 11)	5 + Δ*
12	S	4.2	STU-R	3392	32-TCPAM	Symmetric	49 SHDSL sym 2304 (Case 11)	5 + Δ*
13	S	5.0	STU-C	2560	32-TCPAM	Symmetric	49 SHDSL sym 2048 (Case 16)	5 + Δ*
14	S	5.0	STU-R	2560	32-TCPAM	Symmetric	49 SHDSL sym 2048 (Case 16)	5 + Δ*
15	S	2.3	STU-C	5696	32-TCPAM	Symmetric	24 FDD ADSL + 24 HDSL (Case 6)	5 + Δ*
16	BT1-C	1.9	STU-C	5696	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 4)	5 + Δ*
17	BT1-R	1.9	STU-R	5696	32-TCPAM	Symmetric	24 HDSL2 + 24 T1 (Case 14)	5 + Δ*
18	BT2-C	3.9	STU-C	2560	32-TCPAM	Symmetric	49 HDSL sym 2048 (Case 16)	5 + Δ*
19	BT2-R	3.9	STU-R	2560	32-TCPAM	Symmetric	49 HDSL sym 2048 (Case 16)	5 + Δ*

NOTE – The crosstalk scenarios listed in this table were developed under the assumption of a 50 pair cable binder. Cable binders of other sizes are for further study.

* The indicated noise margins in Table F.4 shall have a tolerance of 1.25 dB due to the aggregate effect of crosstalk generator tolerance and calibrated loop simulator tolerance. The offset Δ is defined in A.3.1.4.

All interferers are assumed to be co-located. All interferer PSDs are described in A.3.3.9. The disturbers used for these tests are identical to those used in Annex A. For example, test 1 in Table F.4 uses the identical disturber shape as case 4 from Annex A, exactly as described by PSD_{Case-4} in A.3.3.9.

F.6 Functional characteristics

Functional characteristics return loss, Span Powering, Longitudinal Balance, and Longitudinal Output Voltage shall be as described in A.5.

Annex G

Reserved for Region 2 requirements for data rates between 2320 kbit/s and **max rate**

Annex H

Deactivation and warm-start procedure

Support of the reduced power mode, the deactivation and the warm-start is optional.

NOTE – Frequent transitions to/from the reduced power mode introduce a non-stationary noise environment, the effect of which on deployed xDSL systems is not fully known. Because of this, regional access restrictions regarding this procedure might apply.

H.1 Deactivation to reduced power mode

This clause describes waveforms at the loop interface and associated procedures during deactivation. Figure H.1 illustrates the deactivation sequence.

H.1.1 Deactivation sequence

The deactivation can be initiated by the STU-R or by the STU-C. EOC signalling is used to initiate the deactivation. The initiating side is called unit A, the other side is called unit B.

The standard sequence is as follows: Upon receiving the EOC message "Deactivation Request", unit B responds by the EOC message "Deactivation Response" or by "Generic Unable To Comply (UTC)". After sending the "Deactivation Response" containing an acceptance to the deactivation (Deactivation Acknowledge bit = "1"), unit B continues transmitting and waits for the deactivation of unit A. After receiving the acceptance to the deactivation request, unit A stops transmitting and enters the reduced power mode. After detecting that unit A has stopped transmitting, e.g., by detecting an LOSW error, unit B stops transmitting and enters the reduced power mode as well.

The EOC messages "Deactivation Request" and "Deactivation Response" indicate the ability of the sender for the deactivation to the reduced power mode and a subsequent warm-start.

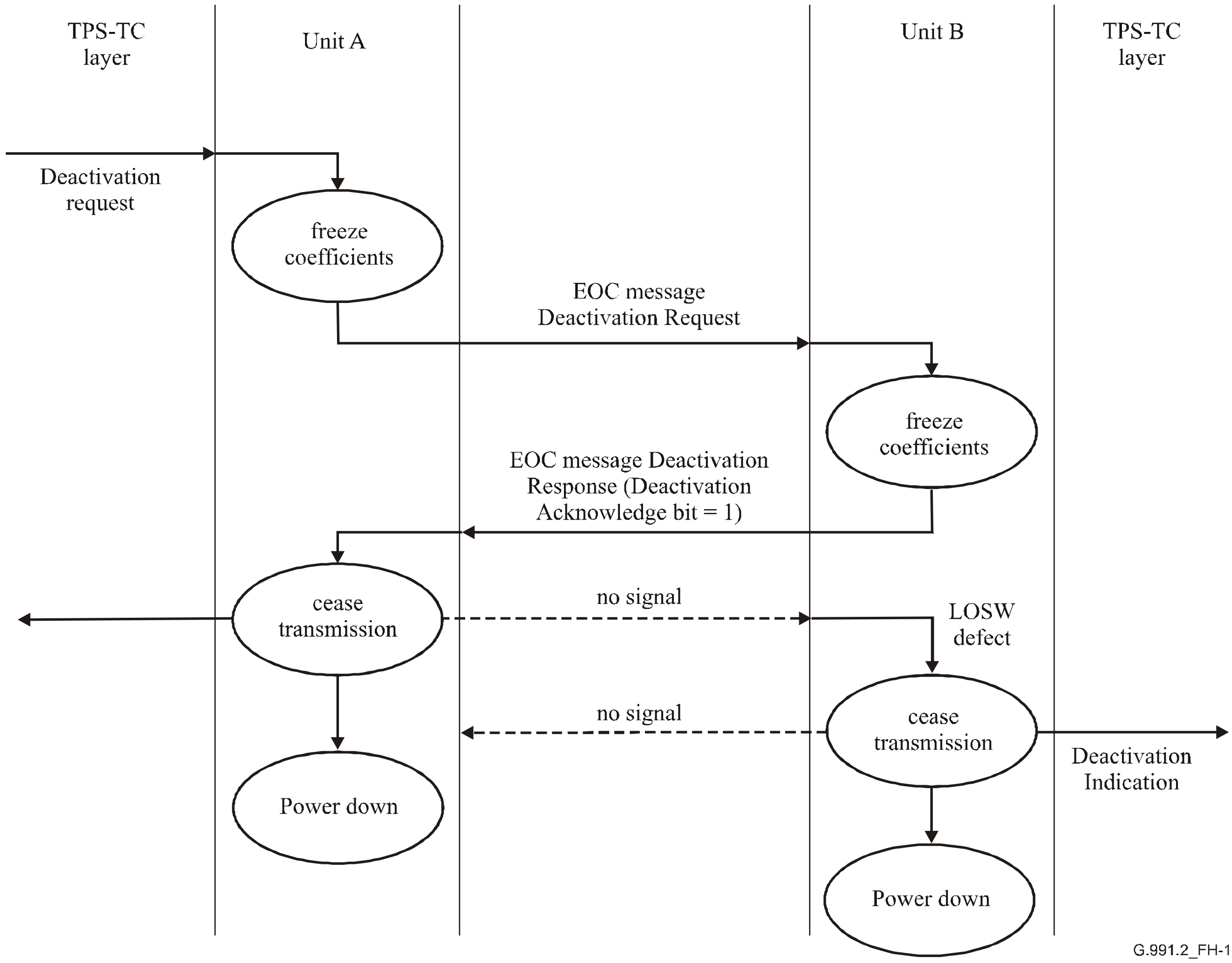


Figure H.1/G.991.2 – Deactivation sequence

H.1.2 Deactivation inhibiting

With messages "Deactivation Request" and "Deactivation Acknowledge", however, each transceiver can also inhibit or stop an initiated deactivation process by setting bit OK to "0" in the relevant EOC message. This is useful when during or after the transmission of the "Deactivation Request" it becomes apparent that the data link is about to be used.

In warm-start the transmission shall be active for at least time t_{active} to minimize effects of non-stationary crosstalk to systems sharing the same binder.

H.1.3 Deactivation EOC messages

H.1.3.1 Deactivation Request message: Message ID 22

The Deactivation Request message is transmitted to request a deactivation or to withdraw an issued deactivation request. The destination address shall be F_{16} to indicate this is a broadcast message.

Table H.1/G.991.2 – Deactivation Request

Octet #	Contents	Data type	Reference
1	22	Message ID	
2 bits 7..1	Reserved		Set to 0
2 bit 0	Deactivation Request	Bit	0 = Deactivation request 1 = Deactivation request cancelled
3	Reserved		Set to 0

H.1.3.2 Deactivation Response Message: Message ID 150

The deactivation response message is used to confirm the deactivation command or to refuse a deactivation request.

Table H.2/G.991.2 – Deactivation Acknowledge

Octet #	Contents	Data type	Reference
1	150	Message ID	
2 bits 7..1	Reserved		Set to 0
2 bit 0	Deactivation Acknowledge	Bit	0 = Deactivation OK 1 = Deactivation not possible
3	Reserved		Set to 0

H.2 Warm-start activation

The warm-start can be initiated by the STU-R or the STU-C. This clause describes waveforms at the loop interface and associated procedures during warm-start. The direct specification of the performance of individual receiver elements is avoided when possible. Instead, the transmitter characteristics are specified on an individual basis and the receiver performance is specified on a general basis as the aggregate performance of all receiver elements. Exceptions are made for cases where the performance of an individual receiver element is crucial to inter-operability.

In contrast to the activation described in 6.2, a warm-start makes use of all settings stored in a previous successful activation to achieve a minimum start-up time. An activation is successful if convergence has been achieved and the data mode has been reached (see 6.1). All settings (i.e., negotiated configuration in the pre-activation, all data in the activation frame, and all values in adaptive filters) have to be stored before deactivating the transmission. The warm-start relies on the fact that all previously stored settings such as the transfer characteristics of the receive and transmit path and the timing relation between receive and transmit signals are still relevant. Small changes (e.g., due to variations of ambient temperature) should not inhibit the warm-start activation; however, if the equipment or the loop characteristics have changed significantly, the warm-start activation may fail, and a cold-start will be performed instead.

H.2.1 Warm-start activation PMD reference model

The block diagram of the warm-start activation PMD layer of an STU-C and STU-R transmitter is shown in Figure H.2.

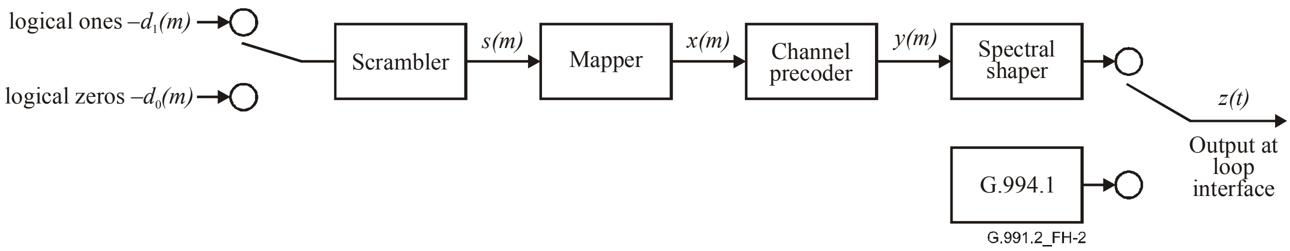


Figure H.2/G.991.2 – Warm-start activation PMD reference model

The time index *m* represents the symbol time, and *t* represents analogue time. Since activation uses 2-PAM modulation, the bit time is equivalent to the symbol time. The output of the scrambler is $s(m)$. The output of the mapper is $y(m)$, and the output of the spectral shaper at the loop interface is $z(t)$. $d_1(m)$ is an initialization signal that shall be logical ones for all m. $d_0(m)$ is an initialization signal that shall be logical zeros for all m. The modulation format shall be Tomlinson-coded 2-level signal, with the full symbol rate selected for data mode operation. During activation, the timing reference for the activation signals have a tolerance of ±32 ppm at the STU-C and ±100 ppm at the STU-R.

The output bits from the scrambler $s(m)$ shall be mapped to an output level $y(m)$ as follows:

Table H.3/G.991.2 – Bit-to-level mapping

Scrambler output $s(m)$	Mapper output level $y(m)$	Data mode index
0	–9/16	0011
1	+9/16	1000

The levels corresponding to a 0 and 1 at the output of the scrambler shall be identical to the levels of the 16-TCPAM constellation corresponding to indexes 0011 and 1000 respectively.

H.2.2 Warm-start activation sequence

The sequence and timing diagram for the warm-start activation sequence is given in Figure H.3.

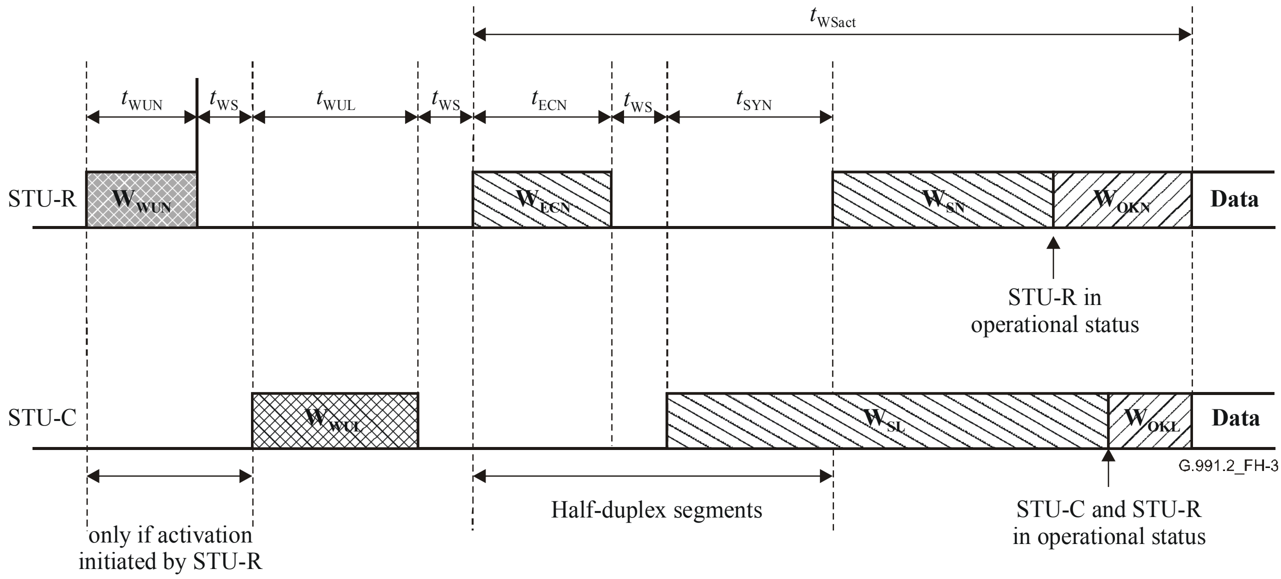


Figure H.3/G.991.2 – Timing diagram for the warm-start activation sequence

Table H.4/G.991.2 – Durations and tolerances for activation signals

Signal	Parameter	Reference	Nominal value	Tolerance
t_{WUN}	Duration of W_{WUN}	H.2.4.1	12 ms	±2 ms
t_{WS}	Guard time to prevent overlapping signals		6 ms	±2 ms
t_{WUL}	Duration of W_{WUL}	H.2.4.2	20 ms	±2 ms
t_{ECN}	Duration of the half-duplex segment of the STU-R	H.2.4.3	40 ms	±2 ms
t_{SYN}	Minimum Duration of the half-duplex segment of the STU-C		100 ms	±2 ms
t_{WSact}	Maximum activation time		500 ms	
t_{active}	Minimum time the link has to remain active		5 min	
NOTE – The maximum time for activation, occurring after a deactivation without any intervening loopback or powering action and without any change in cable characteristic for a metallic pair cable transmission system is t_{WSact}. This value for activation time is understood as a 95%-value when testing with line models specified for the digital transmission system.				

H.2.3 State Transition Diagram

The state transition diagram for the warm-start activation of the STU-R and the STU-C is given in Figure H.4.

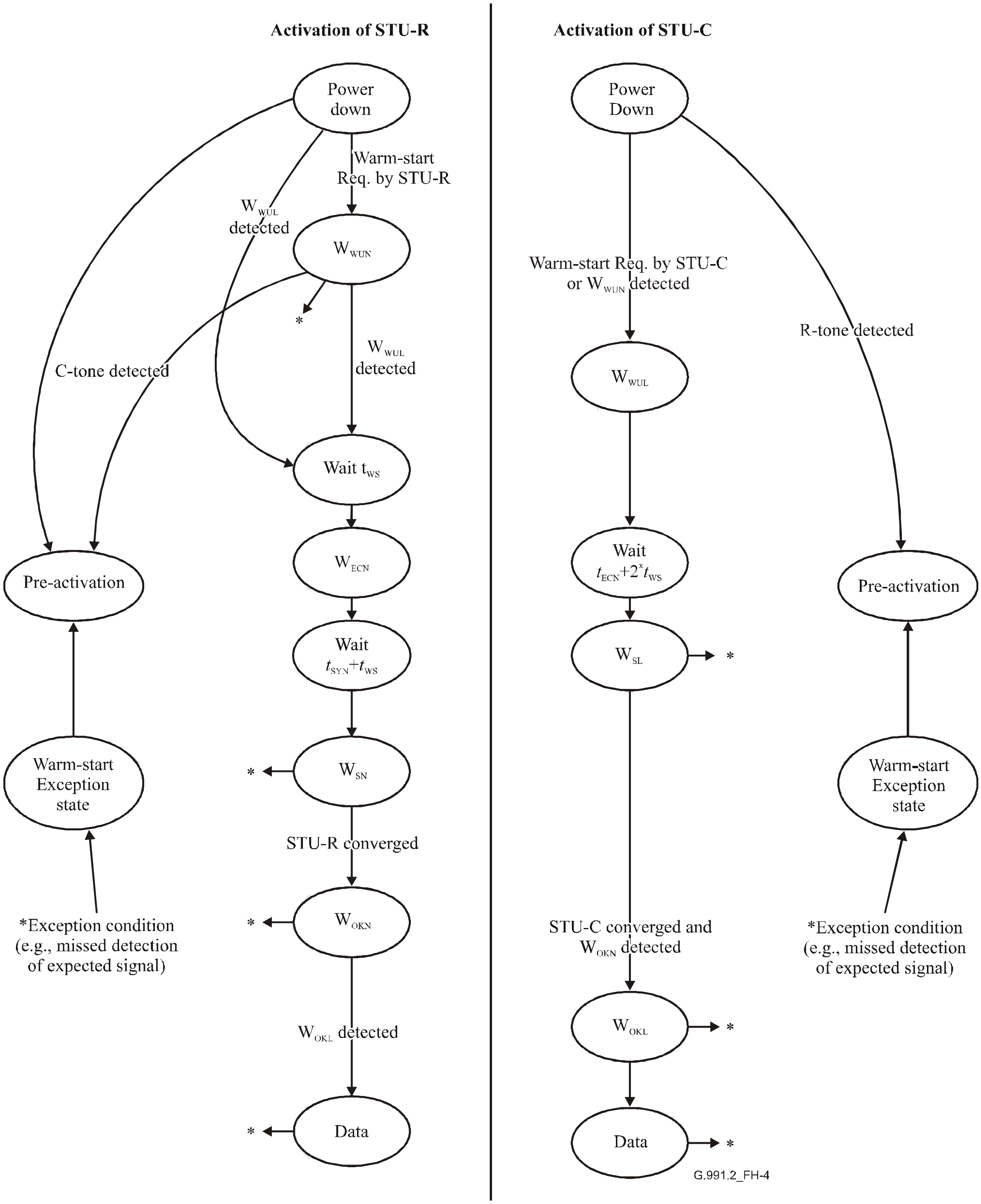


Figure H.4/G.991.2 – STU-C and STU-R transmitter warm-start state transition diagram

H.2.4 Signals used in warm-start activation

H.2.4.1 Signal W_{WUN}

The STU-R initiated warm-start shall start with the STU-R sending the warm-start wake up signal, W_{WUN} for a duration of t_{WUN}. The waveform and the transmit power of W_{WUN} is the same as of the 12 kHz R-Tone used in ITU-T Rec. G.994.1 [2].

H.2.4.2 Signal W_{WUL}

The wake-up signal for the STU-C initiated warm-start shall be the W_{WUL}. If the warm-start is initiated by the STU-R, the STU-C shall send the signal W_{WUL} after detecting the signal W_{WUN}. W_{WUL} shall have a duration of t_{WUL}. The waveform and the transmit power of W_{WUL} is the same as of the 20 kHz C-Tone used in ITU-T Rec. G.994.1 [2].

H.2.4.3 Signal W_{ECN}

The STU-R shall send W_{ECN}, beginning t_{WS} after the end of W_{WUL}. Waveform W_{ECN} shall be generated by connecting logical ones to the input of the STU-R scrambler as shown in Figure H.2. The transmit power, symbol rate and PSD mask for W_{ECN} shall be as for signal W_{SL}.

Half-duplex signal W_{ECN} shall be sent for time t_{ECN}.

H.2.4.4 Signal W_{SL}

The STU-C shall send W_{SL} beginning t_{WS} after the end of W_{ECN}. Waveform W_{SL} shall be generated by connecting logical ones to the input of the STU-C scrambler as shown in Figure H.2. The transmit power, symbol rate and PSD mask for W_{SL} shall be as negotiated during the pre-activation sequence.

H.2.4.5 Signal W_{SN}

The STU-R shall start transmitting W_{SN} beginning $t_{WS} + t_{SYN}$ after the end of W_{ECN}. Waveform W_{SN} shall be generated by connecting logical ones to the input of the STU-R scrambler as shown in Figure H.2. The transmit power, symbol rate and PSD mask for W_{SN} shall be as negotiated during the pre-activation sequence.

H.2.4.6 Signal W_{OKN}

The STU-R shall start transmitting W_{OKN} when the STU-R achieves full operational status. Full operational status of the STU-R means that the STU-R is ready to enter data mode. Waveform W_{OKN} shall be generated by connecting logical zeros to the input of the STU-R scrambler as shown in Figure H.2. The transmit power, symbol rate and PSD mask for W_{OKN} shall be as for signal W_{SN}.

H.2.4.7 Signal W_{OKL}

The STU-C shall send W_{OKL} when the STU-C has both detected W_{OKL} and achieves full operational status. Full operational status of the STU-C means that the STU-C is ready to enter data mode. Waveform W_{OKL} shall be generated by connecting logical zeros signal to the input of the STU-C scrambler as shown in Figure H.2. The transmit power, symbol rate and PSD mask for W_{OKL} shall be the same as for W_{SL}. W_{OKL} shall be sent for exactly 256 symbols.

H.2.4.8 $Data_c$ and $Data_r$

Within 200 symbols after the end of W_{OKL}, the STU-C shall send $Data_c$ and STU-R shall send $Data_r$. These signals are described in 6.2.2.7. There is no required relationship between the end of W_{OKL} and any bit within the SHDSL data-mode frame. The SHDSL payload data shall be valid $T_{payloadValid}$ (see Table H.5) after the end of W_{OKL}.

H.2.4.9 Warm-start exception condition

An exception condition shall be declared during warm-start if the timeout values given in Table H.5 expire or if any vendor-defined abnormal event occurs.

H.2.4.10 Warm-start exception state

If an exception condition is declared during warm-start, the STU-C or STU-R enters the exception state and warm-start is aborted. During the exception state, the STU shall be silent for at least $T_{silence}$ (see Table H.5), wait for transmission from the far end to cease, then return to the corresponding initial start-up state. The STU-R and STU-C shall begin pre-activation, as per 6.3.

H.2.4.11 Timeouts

Table H.5 shows the system timeouts and their values.

Table H.5/G.991.2 – Timeout values

Name	Parameter	Value
$T_{silence}$	Minimum time in the warm-start exception state where the STU-C or STU-R are silent before the start of pre-activation.	See Table 6-3
$T_{payloadValid}$	Time from start of $Data_c$ or $Data_r$ to valid SHDSL payload data	See Table 6-3

Appendix I

Test circuit examples

I.1 Example crosstalk injection test circuit

Figure I.1 is an example of a high-impedance crosstalk injection circuit.

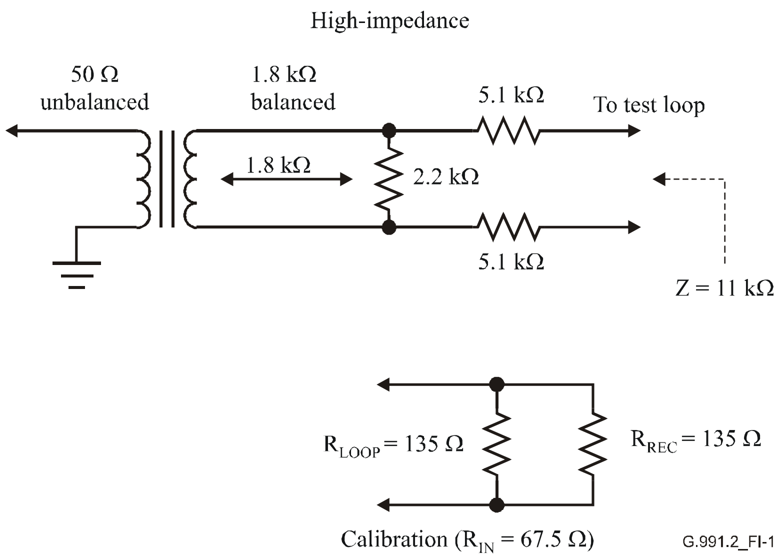


Figure I.1/G.991.2 – Example high-impedance crosstalk injection circuit

I.2 Example coupling circuits for longitudinal balance and longitudinal output voltage

Longitudinal balance and longitudinal output voltage may be measured using the coupling circuits described in ANSI/IEEE Standard 455-1985 [B7] and ITU-T Rec. O.9 [B8]. The coupling circuit in Figure I.2 is based upon the measurement method defined in ANSI/IEEE Standard 455-1985. In order to provide sufficient measurement resolution the resistors must be matched within 0.05 % tolerance. The coupling circuit in Figure I.3 is based on the measurement method described in ITU-T Rec. O.9. This test circuit uses precision balanced (bifilar wound) transformers/baluns and does not require precision matched resistors. The balun circuit is often more convenient for high-frequency measurements.

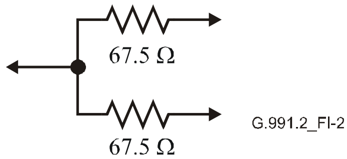


Figure I.2/G.991.2 – Example resistive coupling circuit

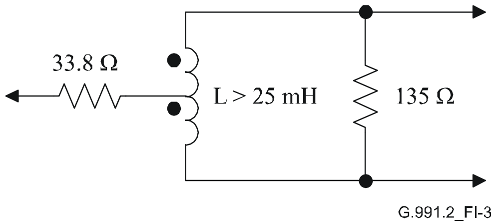


Figure I.3/G.991.2 – Example balun coupling circuit

I.3 Return loss test circuit

The test circuit in Figure I.4 is based upon the traditional return loss bridge with added components to accommodate the DC power feed voltage and provide transformer isolation for the measurement instrumentation. Transformer isolation of both test signal source and meter load prevent measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. Input V_{IN} is connected to a sweeping sine wave generator (50 Ω source) and V_{OUT} is connected to a high-impedance frequency selective voltmeter (or spectrum analyser). For this test circuit, the return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{Z_{TEST}(f)+Z_{REF}}{Z_{TEST}(f)-Z_{REF}}\right|$$

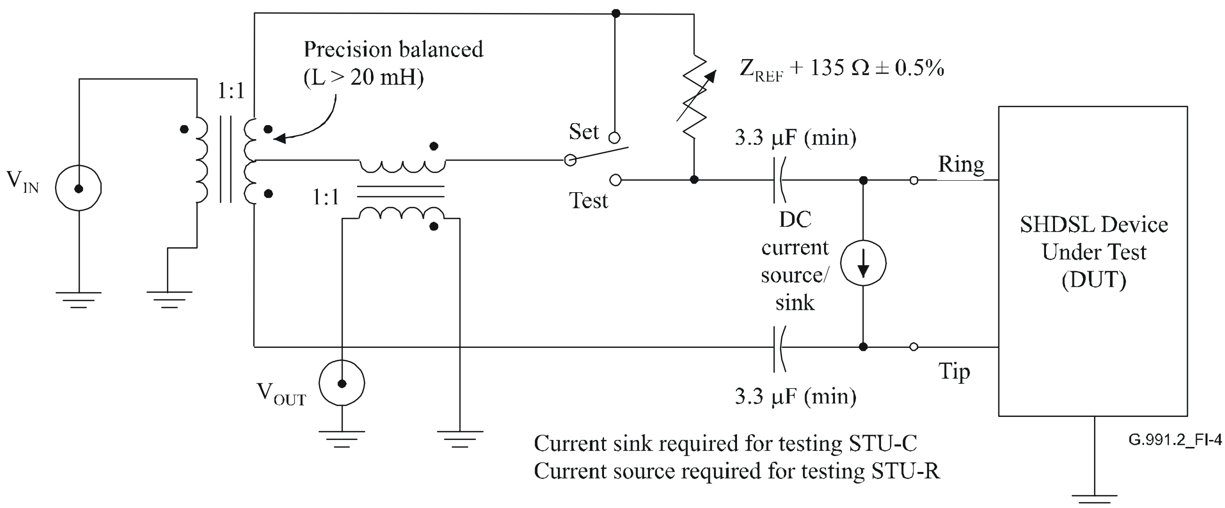


Figure I.4/G.991.2 – Example return loss bridge test circuit (ground isolated)

I.4 Transmit PSD/total power measurement test circuit

The test circuit in Figure I.5 is designed to measure total transmit power and transmit PSD. The test contains provisions for DC power feed and transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. V_{OUT} is connected to a high-impedance wideband rms voltmeter (or spectrum analyser).

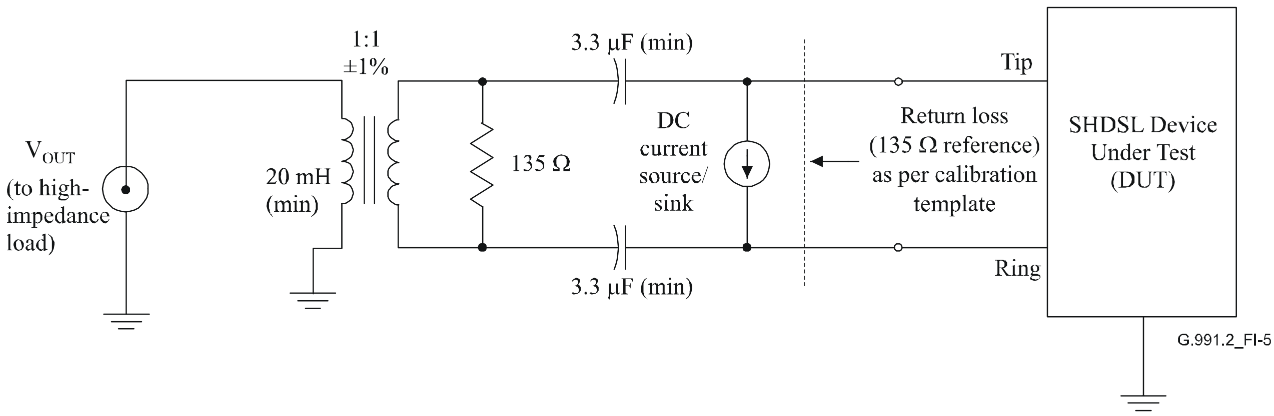


Figure I.5/G.991.2 – Example ground-isolated power/PSD measurement test circuit

Appendix II

Typical characteristics of cables

II.1 Typical characteristics of cables for Annex B

NOTE – Parameters in this appendix differ from those specified in ITU-T Rec. G.996.1 [B11] for PE 04 and PE 05 cable.

Table II.1/G.991.2 – PE cable constants

	PE04			PE05			PE06			PE08		
freq [Hz] $\times 10^3$	**Rs [Ω/m] $\times 10^{-3}$**	**Ls [H/m] $\times 10^{-9}$**	**Cp [F/m] $\times 10^{-12}$**	**Rs [Ω/m] $\times 10^{-3}$**	**Ls [H/m] $\times 10^{-9}$**	**Cp [F/m] $\times 10^{-12}$**	**Rs [Ω/m] $\times 10^{-3}$**	**Ls [H/m] $\times 10^{-9}$**	**Cp [F/m] $\times 10^{-12}$**	**Rs [Ω/m] $\times 10^{-3}$**	**Ls [H/m] $\times 10^{-9}$**	**Cp [F/m] $\times 10^{-12}$**
0	268	680	45.5	172	680	25	119	700	56	67	700	37.8
10	268	678	45.5	172	678	25	120	695	56	70.0	700	37.8
20	269	675	45.5	173	675	25	121	693	56	72.5	687	37.8
40	271	669	45.5	175	667	25	125	680	56	75.0	665	37.8
100	282	650	45.5	190	646	25	146	655	56	91.7	628	37.8
150	295	642	45.5	207	637	25	167	641	56	105	609	37.8
200	312	635	45.5	227	629	25	189	633	56	117	595	37.8
400	390	619	45.5	302	603	25	260	601	56	159	568	37.8
500	425	608	45.5	334	592	25	288	590	56	177.5	560	37.8
700	493	593	45.5	392	577	25	340	576	56	209	553	37.8
1000	582	582	45.5	466	572	25	405	570	56	250	547	37.8
2000	816	571	45.5	655	565	25	571	560	56	353	540	37.8

Table II.2/G.991.2 – PVC cable constants

		PVC032				PVC04				PVC063		
freq [Hz] × 10^3		Rs [Ω/m] × 10^{-3}	Ls [H/m] × 10^{-9}	Cp [F/m] × 10^{-12}		Rs [Ω/m] × 10^{-3}	Ls [H/m] × 10^{-9}	Cp [F/m] × 10^{-12}		Rs [Ω/m] × 10^{-3}	Ls [H/m] × 10^{-9}	Cp [F/m] × 10^{-12}
0		419	650	120		268	650	120		108	635	120
10		419	650	120		268	650	120		108	635	120
20		419	650	120		268	650	120		108	635	120
40		419	650	120		268	650	120		111	630	120
100		427	647	120		281	635	120		141	604	120
150		453	635	120		295	627	120		173	584	120
200		493	621	120		311	619	120		207	560	120
400		679	577	120		391	592	120		319	492	120
500		750	560	120		426	579	120		361	469	120
700		877	546	120		494	566	120		427	450	120
1000		1041	545	120		584	559	120		510	442	120
2000		1463	540	120		817	550	120		720	434	120

Appendix III

Signal regenerator start-up description

This appendix describes the start-up sequence used on spans employing regenerators. The sequence applies to spans with an arbitrary number of regenerators (up to 8), but for simplicity, the description here assumes a two-regenerator link. The use of line probing is optional, but its use is assumed for the purpose of this description.

The basic premise is that capability lists and line probe results propagate from the STU-R toward the STU-C and that the SHDSL training begins at the STU-C and propagates in the direction toward the STU-R. The Regenerator Silent Period (RSP) bit in ITU-T Rec. G.994.1 is used to hold off segments while the start-up process propagates across the span.

The block diagram in Figure III.1 shows a typical SHDSL span with two regenerators as a reference for the start-up sequences described below.

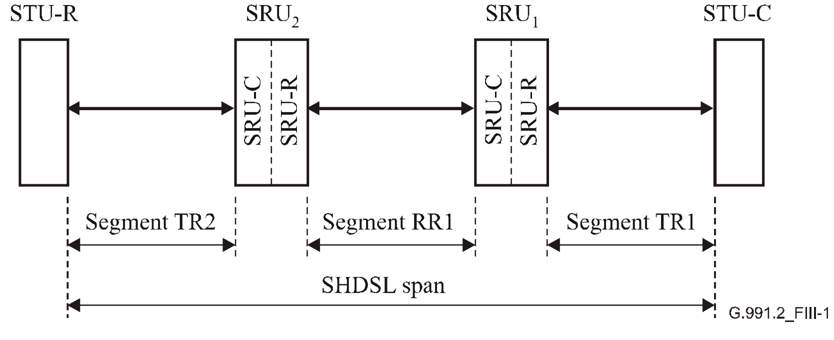


Figure III.1/G.991.2 – Block diagram of a SHDSL span with two signal regenerators

III.1 STU-R initiated Start-up

In most typical SHDSL installations, the STU-R can be expected to initiate the start-up process. The proposed SHDSL start-up process for STU-R initiation is described in the text below and shown graphically in Table III.1.

In this mode, the STU-R triggers the start-up process by initiating a G.994.1 session with the regenerator closest to it (over segment TR2). The STU-R and the SRU_2-C then exchange capabilities and optionally perform a line probe and a second capabilities exchange. The units do not have enough information to begin SHDSL activation at this point, so the SRU_2-C issues an MS with the RSP bit set to hold off the STU-R while the start-up process propagates across the span. The G.994.1 session terminates normally, and the STU-R begins its waiting period.

Next, the SRU_2-C conveys the capabilities from Segment TR2 to the SRU_2-R across the regenerator's internal interface. The SRU_2-R then initiates a G.994.1 session with the SRU_1-C and performs the same capabilities exchange and line probing sequence described above for the first segment. The capabilities expressed by the SRU_2-R are the intersection of its own capabilities with the capabilities it has received for Segment TR2. The units still do not have sufficient information to begin SHDSL activation, so, again, the SRU_1-R issues an MS with the RSP bit set. The G.994.1 session terminates normally, and the SRU_2-R begins its waiting period.

As before, the SRU_1-C then conveys the capabilities from Segment RR1 (including the information from Segment TR2) to the SRU_1-R across the regenerator's internal interface. The SRU_1-R initiates a G.994.1 session with the STU-C and performs a capabilities exchange. Optionally, a line probe and a second capabilities exchange may be used. As before, the capabilities expressed by the SRU_1-R are the intersection of its own capabilities with the capabilities it has received for Segments RR1 and TR2. At this point, the STU-C possesses all of the required information to select the span's operational parameters. The data rate and other parameters are selected, just as in a normal (non-regenerator) pre-activation sequence and then the SHDSL activation begins for Segment TR1.

When the STU-C/SRU_1-R link (over Segment TR1) has completed the SHDSL activation sequence (or the G.994.1 session, if clock mode 1 is selected), the SRU_1-R communicates the selected operational parameters to the SRU_1-C across the regenerator's internal interface. At this point, the SRU_1-C initiates a G.994.1 session with the SRU_2-R over Segment RR1. Parameters are selected – there should be no need for another CLR-CL exchange at this point – and the units perform the normal SHDSL activation. If clock mode 1 is selected (classic plesiochronous), there is no need to lock symbol timing to a network clock reference. In this case, the SRU_1-C/SRU_2-R G.994.1 session and activation should begin as soon as the STU-C/SRU_1-R G.994.1 sessions complete. In clock modes 2, 3a, and 3b, such a network or data clock reference is necessary for establishing symbol timing. In these modes, the SRU_1-C will delay the initiation of its G.994.1 session until the STU-C/SRU_1-R activation is complete. In this way, the required reference clock will be available for symbol timing on the SRU_1-C/SRU_2-R segment.

When the SRU_1-C/SRU_2-R link (over Segment RR1) has completed the SHDSL activation sequence (or the G.994.1 session, if clock mode 1 is selected), the SRU_2-R communicates the selected operational parameters to the SRU_2-C across the regenerator's internal interface. The SRU_2-C initiates a G.994.1 session with the STU-R over Segment TR2. Parameters are selected and the units perform the normal SHDSL activation. When this activation sequence is complete, the span can become fully operational.

Table III.1/G.991.2 – STU-R initiated start-up sequence

Segment TR2 (STU-R/SRU_2-C)	Segment RR1 (SRU_2-R/SRU_1-C)	Segment TR1 (SRU_1-R/STU-C)
G.994.1 Start → Capabilities exchange *Line probe* *Capabilities exchange* ← MS (RSP)		
	G.994.1 Start → Capabilities exchange *Line probe* *Capabilities exchange* ← MS (RSP)	
		G.994.1 Start → Capabilities exchange *Line probe* *Capabilities exchange* Mode Selection SHDSL activation
	← G.994.1 Start Mode Selection SHDSL activation	
← G.994.1 Start Mode Selection SHDSL activation		

III.2 STU-C initiated start-up

In some cases, it may be desirable for the STU-C to initiate the start-up process. The proposed SHDSL start-up process for STU-C initiation is described in the text below and shown graphically in Table III.2.

In this mode, the STU-C triggers the start-up process by initiating a G.994.1 session with the regenerator closest to it (over segment TR1). The SRU_2-C issues an MS with the RSP bit set to hold off the STU-C while the start-up process propagates across the span. The G.994.1 session terminates normally, and the STU-C begins its wait period. Next, the SRU_1-C initiates a G.994.1 session with the SRU_2-R, which, again is terminated following an MS from the SRU_2-R with the RSP bit set.

The SRU_2-C next initiates a G.994.1 session with the STU-R. From this point on, the start sequence is as described in III.1 for the STU-R initiated start-up.

Table III.2/G.991.2 – STU-C initiated start-up sequence

Segment TR2 (STU-R/SRU_2-C)	Segment RR1 (SRU_2-R/SRU_1-C)	Segment TR1 (SRU_1-R/STU-C)
		← G.994.1 Start
		MS (RSP) →
	← G.994.1 Start	
	MS (RSP) →	
← G.994.1 Start		
Capabilities exchange		
Line probe		
Capabilities exchange		
← MS (RSP)		
	G.994.1 Start →	
	Capabilities exchange	
	Line probe	
	Capabilities exchange	
	← MS (RSP)	
		G.994.1 Start →
		Capabilities exchange
		Line probe
		Capabilities exchange
		Mode Selection
		SHDSL activation
	← G.994.1 Start	
	Mode Selection	
	SHDSL activation	
← G.994.1 Start		
Mode Selection		
SHDSL activation		

III.3 SRU initiated start-up

In some limited applications (including some maintenance and retrain scenarios), it may be desirable for a regenerator to initiate the start sequence. In this mode, the SRU will initiate the train in the downstream direction – i.e., toward the STU-R in the same manner that it would have for the corresponding segment of the STU-C Start-up Procedure (as described in III.2). The STU-R will then initiate the capabilities exchange and line probing procedure toward the STU-C, as in a normal STU-C initiated start-up. The start-up sequence begins with the initiating SRU-C and propagating toward the STU-R.

III.4 Collisions and retrains

Collisions (equivalent to "glare" conditions in voice applications) can occur in cases where both the STU-C and the STU-R attempt to initiate connections simultaneously. Using the process described above, these collisions are resolved by specifying that R-to-C capabilities exchanges and probes will always take precedence over C-to-R train requests. G.994.1 sessions inherently resolve collisions on individual segments.

In ITU-T Rec. G.994.1, the RSP timeout is specified as approximately 1 minute. For spans with no more than one regenerator, this is ideal. For multi-regenerator spans, however, an STU may time out and initiate a new G.994.1 session before the SRU is prepared to begin the next phase of the train. In such cases, the SRU should respond to the G.994.1 initiation and issue an MS message with the RSP bit set to hold off the STU once again. For its part, the SRU should implement an internal timer and should not consider a start-up to have failed until that timer has expired. The timer should be started when the SRU receives a RSP bit in an MS message and should not expire for at least 4 minutes.

If any segment must retrain due to line conditions or other causes, each segment of the span shall be deactivated and the full start-up procedure shall be reinitiated.

III.5 Diagnostic mode activation

If a segment fails, the start-up procedure will also fail for the entire span. This would normally be characterized at the STU by being told to enter a silent interval via the RSP bit and never receiving another G.994.1 request. Without some diagnostic information, the service provider would have no easy way to test the integrity of the various segments.

This concern is resolved by the use of the "Diagnostic Mode" in ITU-T Rec. G.994.1 to trigger a diagnostic training mode. This bit, when set, causes an SRU connected to a failed segment to act as an STU and allow the start-up procedure to finish. In this way, all of the segments before the failed segment may be tested using loopbacks and EOC-initiated tests, allowing network operators to quickly isolate the segment where the failure has occurred.

Appendix IV

Tabulation of Annex B noise profiles

Appendix IV tabulates the total noise profile (sum of self and alien) corresponding to 0 dB of margin for all the Annex B test cases. Those noise PSDs were used during the theoretical computation of the margin. The tabulated noise profiles should be measured into the calibrating impedance (see B.3.3.1).

Noise Profile Nomenclature: ABBBCDE

A: Side (either C or R)

BBB: Rate

C: PSD type (either s for symmetric or a for asymmetric)

D: Noise Type (A ,B, C or D)

E: Loop Number (from 2 to 7).

The noise shapes used for test #1 will be identical to Noise A of test #2

Table IV.1/G.991.2 – STU-C side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
C384sA2	114.9	99.2	95.0	93.1	92.5	92.3	92.9	93.9	93.4	92.7	92.0	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C384sC2	120.6	104.6	100.4	98.4	97.7	97.6	98.7	101.8	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C384sD2	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C512sA2	114.9	99.4	95.3	93.4	92.8	92.3	92.0	91.9	92.0	92.2	91.9	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C512sC2	120.6	104.9	100.8	98.8	98.1	97.7	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C512sD2	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C768sA2	114.9	99.6	95.6	93.7	93.3	92.8	92.4	91.9	91.2	90.7	90.3	88.1	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C768sC2	120.6	105.2	101.2	99.3	98.8	98.4	98.0	97.5	97.0	96.6	96.4	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C768sD2	134.2	107.3	102.2	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
C1024sA2	114.9	99.7	95.7	93.9	93.6	93.2	92.8	92.3	91.5	90.8	90.3	87.5	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C1024sC2	120.6	105.3	101.4	99.6	99.2	99.0	98.7	98.2	97.5	96.9	96.4	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1024sD2	135.0	108.5	103.3	100.6	98.8	97.5	96.4	95.5	94.9	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
C1280sA2	114.9	99.7	95.8	93.9	93.8	93.5	93.1	92.6	91.8	91.1	90.4	87.3	86.0	84.9	83.8	82.9	82.1	79.4	77.6
C1280sC2	120.6	105.4	101.5	99.7	99.5	99.4	99.3	98.8	98.0	97.4	96.8	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.8
C1280sD2	135.7	109.4	104.3	101.5	99.7	98.3	97.2	96.3	95.5	94.9	94.4	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
C1536sA2	115.0	99.7	95.8	94.0	93.8	93.6	93.3	92.8	92.0	91.2	90.6	87.3	85.8	84.7	83.8	82.9	82.1	79.4	77.6
C1536sC2	120.6	105.4	101.5	99.8	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.3	91.9	91.1	90.2	89.3	88.5	87.8	86.8
C1536sD2	136.1	110.2	105.0	102.3	100.4	99.0	97.9	96.9	96.1	95.5	94.9	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0
C2048sA2	115.0	99.7	95.7	93.9	93.8	93.6	93.3	92.8	91.9	91.2	90.5	87.2	85.5	84.3	83.5	82.8	82.1	79.4	77.6
C2048sC2	120.6	105.4	101.5	99.8	99.6	99.7	99.7	99.4	98.5	97.8	97.2	93.1	91.6	90.4	89.7	89.2	88.5	87.8	86.8
C2048sD2	136.3	110.4	105.2	102.5	100.6	99.1	98.0	97.0	96.2	95.5	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
C2304sA2	115.0	99.7	95.8	94.0	93.8	93.6	93.4	92.9	92.0	91.2	90.6	87.2	85.5	84.3	83.4	82.7	82.0	79.4	77.6
C2304sC2	120.6	105.4	101.5	99.8	99.7	99.9	100.0	99.7	98.8	98.1	97.4	93.2	91.6	90.4	89.5	88.9	88.4	87.8	86.8
C2304sD2	136.6	110.9	105.7	102.9	101.0	99.6	98.4	97.4	96.6	95.9	95.3	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0

Table IV.1/G.991.2 – STU-C side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
C384sD3	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C512sD3	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C768sD3	134.1	107.3	102.2	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
C1024sD3	135.0	108.5	103.3	100.6	98.8	97.4	96.4	95.5	94.8	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
C1280sD3	135.6	109.4	104.2	101.5	99.7	98.3	97.2	96.2	95.5	94.9	94.3	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
C1536sD3	136.1	110.1	105.0	102.3	100.4	99.0	97.8	96.9	96.1	95.4	94.8	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0
C2048sD3	136.3	110.3	105.2	102.4	100.5	99.1	97.9	96.9	96.1	95.4	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
C2304sD3	136.6	110.8	105.6	102.9	101.0	99.5	98.3	97.4	96.5	95.8	95.2	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0
C384sA4	114.9	99.2	95.0	93.1	92.5	92.3	92.9	93.9	93.4	92.7	92.0	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C384sC4	120.6	104.6	100.4	98.4	97.7	97.6	98.7	101.8	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C512sA4	114.9	99.4	95.3	93.4	92.8	92.3	92.0	91.9	92.0	92.2	91.9	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C512sC4	120.6	104.9	100.8	98.8	98.1	97.7	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C768sA4	114.9	99.5	95.6	93.7	93.3	92.8	92.4	91.8	91.2	90.6	90.3	88.0	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C768sC4	120.6	105.2	101.2	99.3	98.7	98.4	98.0	97.5	97.0	96.6	96.4	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1024sA4	114.9	99.6	95.7	93.8	93.6	93.2	92.8	92.2	91.5	90.8	90.2	87.5	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C1024sC4	120.6	105.3	101.4	99.6	99.2	99.0	98.7	98.2	97.5	96.9	96.4	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1280sA4	114.9	99.6	95.7	93.9	93.7	93.4	93.1	92.5	91.7	91.0	90.4	87.3	86.0	84.9	83.8	82.9	82.1	79.4	77.6
C1280sC4	120.6	105.3	101.5	99.7	99.4	99.4	99.2	98.8	98.0	97.3	96.8	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.8
C1536sA4	114.9	99.6	95.7	93.9	93.8	93.5	93.2	92.7	91.9	91.2	90.5	87.3	85.8	84.7	83.8	82.9	82.1	79.4	77.6
C1536sC4	120.6	105.3	101.5	99.8	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.3	91.9	91.1	90.2	89.3	88.5	87.8	86.8
C2048sA4	115.0	99.6	95.6	93.9	93.7	93.5	93.2	92.6	91.8	91.0	90.4	87.1	85.5	84.3	83.5	82.8	82.1	79.4	77.6
C2048sC4	120.6	105.3	101.4	99.7	99.6	99.7	99.7	99.3	98.4	97.7	97.1	93.1	91.5	90.4	89.7	89.2	88.5	87.8	86.8
C2304sA4	115.0	99.6	95.6	93.9	93.7	93.5	93.2	92.7	91.8	91.1	90.4	87.1	85.4	84.2	83.4	82.7	82.0	79.4	77.6
C2304sC4	120.6	105.3	101.4	99.7	99.6	99.8	99.9	99.5	98.7	98.0	97.3	93.2	91.6	90.4	89.5	88.9	88.4	87.8	86.8

Table IV.1/G.991.2 – STU-C side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
C384sB5	120.4	104.6	100.3	98.4	97.7	97.6	98.7	101.7	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C512sB5	120.4	104.9	100.7	98.8	98.0	97.6	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C768sB5	120.4	105.1	101.1	99.2	98.6	98.3	97.9	97.4	96.9	96.5	96.3	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C1024sB5	120.4	105.2	101.2	99.4	99.0	98.8	98.5	98.0	97.4	96.8	96.3	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C1280sB5	120.4	105.2	101.3	99.5	99.2	99.1	99.0	98.6	97.8	97.2	96.7	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.9
C1536sB5	120.4	105.1	101.2	99.5	99.3	99.3	99.3	98.9	98.2	97.5	97.0	93.2	91.9	91.1	90.2	89.3	88.5	87.8	86.9
C2048sB5	120.4	105.0	101.1	99.3	99.1	99.1	99.1	98.7	97.9	97.3	96.7	93.0	91.5	90.4	89.7	89.2	88.5	87.8	86.9
C2304sB5	120.5	104.9	101.0	99.2	99.0	99.1	99.1	98.8	98.1	97.4	96.8	93.0	91.5	90.4	89.5	88.9	88.4	87.8	86.9
C384sA6	114.9	99.2	95.0	93.1	92.5	92.3	92.9	93.9	93.4	92.7	92.0	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C384sC6	120.6	104.6	100.4	98.4	97.7	97.6	98.7	101.8	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C512sA6	114.9	99.4	95.3	93.4	92.8	92.3	92.0	91.9	92.0	92.2	91.9	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C512sC6	120.6	104.9	100.8	98.8	98.1	97.7	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C768sA6	114.9	99.6	95.6	93.7	93.3	92.9	92.4	91.9	91.2	90.7	90.3	88.0	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C768sC6	120.6	105.2	101.2	99.3	98.8	98.4	98.0	97.5	97.0	96.6	96.4	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1024sA6	115.0	99.7	95.7	93.9	93.6	93.2	92.8	92.3	91.5	90.9	90.3	87.5	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C1024sC6	120.6	105.3	101.4	99.6	99.2	99.0	98.7	98.2	97.5	96.9	96.4	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1280sA6	115.0	99.7	95.8	94.0	93.8	93.5	93.2	92.7	91.9	91.2	90.5	87.3	86.0	84.9	83.8	82.9	82.1	79.4	77.6
C1280sC6	120.6	105.4	101.5	99.7	99.5	99.4	99.3	98.8	98.1	97.4	96.8	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.8
C1536sA6	115.1	99.8	95.8	94.0	93.9	93.7	93.4	92.9	92.1	91.4	90.7	87.3	85.7	84.8	83.8	82.9	82.1	79.4	77.6
C1536sC6	120.6	105.4	101.5	99.8	99.6	99.8	99.8	99.4	98.6	97.9	97.3	93.3	91.9	91.1	90.2	89.3	88.5	87.8	86.8
C2048sA6	115.4	100.0	95.9	94.0	93.9	93.7	93.4	93.0	92.1	91.4	90.7	87.2	85.5	84.4	83.5	82.8	82.1	79.4	77.6
C2048sC6	120.7	105.4	101.5	99.8	99.7	99.8	99.8	99.5	98.6	97.9	97.3	93.1	91.5	90.4	89.7	89.2	88.5	87.8	86.8
C2304sA6	115.6	100.2	96.0	94.1	94.0	93.8	93.6	93.1	92.3	91.5	90.9	87.3	85.5	84.4	83.4	82.7	82.0	79.4	77.6
C2304sC6	120.7	105.4	101.5	99.8	99.7	100.0	100.1	99.8	99.0	98.3	97.6	93.2	91.6	90.4	89.6	88.9	88.4	87.8	86.8

Table IV.1/G.991.2 – STU-C side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
C384sA7	114.9	99.2	95.0	93.1	92.5	92.3	92.9	93.9	93.4	92.7	92.0	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C384sB7	120.6	104.6	100.4	98.4	97.7	97.6	98.7	101.8	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C384sC7	120.6	104.6	100.4	98.4	97.7	97.6	98.7	101.8	102.6	102.0	101.3	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C384sD7	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C512sA7	114.9	99.4	95.3	93.4	92.8	92.3	92.0	91.9	92.0	92.2	91.9	88.1	86.3	85.0	83.8	82.9	82.1	79.4	77.6
C512sB7	120.6	104.9	100.8	98.8	98.1	97.7	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C512sC7	120.6	104.9	100.8	98.8	98.1	97.7	97.4	97.5	98.3	100.0	100.9	94.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C512sD7	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
C768sA7	114.9	99.5	95.6	93.7	93.3	92.8	92.4	91.8	91.2	90.7	90.3	88.1	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C768sB7	120.6	105.2	101.2	99.3	98.7	98.4	98.0	97.5	97.0	96.6	96.4	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C768sC7	120.6	105.2	101.2	99.3	98.7	98.4	98.0	97.5	97.0	96.6	96.4	94.4	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C768sD7	134.1	107.2	102.1	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
C1024sA7	114.9	99.6	95.7	93.8	93.6	93.2	92.8	92.2	91.5	90.8	90.3	87.5	86.3	84.9	83.8	82.9	82.1	79.4	77.6
C1024sB7	120.6	105.3	101.4	99.6	99.2	99.0	98.7	98.2	97.5	96.9	96.4	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.9
C1024sC7	120.6	105.3	101.4	99.6	99.2	99.0	98.7	98.2	97.5	96.9	96.4	93.5	92.7	91.4	90.2	89.3	88.5	87.8	86.8
C1024sD7	135.0	108.4	103.3	100.6	98.8	97.4	96.4	95.5	94.9	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
C1280sA7	114.9	99.6	95.7	93.9	93.7	93.4	93.1	92.6	91.8	91.1	90.4	87.3	86.0	84.9	83.8	82.9	82.1	79.4	77.6
C1280sB7	120.6	105.3	101.5	99.7	99.4	99.4	99.2	98.8	98.0	97.4	96.8	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.9
C1280sC7	120.6	105.3	101.5	99.7	99.4	99.4	99.2	98.8	98.0	97.4	96.8	93.2	92.2	91.3	90.2	89.3	88.5	87.8	86.8
C1280sD7	135.7	109.4	104.2	101.5	99.7	98.3	97.2	96.3	95.5	94.9	94.3	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
C1536sA7	115.0	99.7	95.7	93.9	93.8	93.6	93.3	92.8	91.9	91.2	90.6	87.3	85.8	84.8	83.8	82.9	82.1	79.4	77.6
C1536sB7	120.6	105.3	101.5	99.8	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.3	91.9	91.1	90.2	89.3	88.5	87.8	86.9
C1536sC7	120.6	105.3	101.5	99.8	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.3	91.9	91.1	90.2	89.3	88.5	87.8	86.8
C1536sD7	136.1	110.1	105.0	102.2	100.4	99.0	97.8	96.9	96.1	95.5	94.9	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0

Table IV.1/G.991.2 – STU-C side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	10	20	30	40	50	60	70	80	90	100	150	200	250	300	350	400	600	800
C2048sA7	115.0	99.7	95.7	93.9	93.7	93.5	93.2	92.7	91.9	91.2	90.5	87.2	85.5	84.4	83.5	82.8	82.1	79.4	77.6
C2048sB7	120.6	105.3	101.4	99.7	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.1	91.6	90.4	89.7	89.2	88.5	87.8	86.9
C2048sC7	120.6	105.3	101.4	99.7	99.6	99.7	99.7	99.3	98.5	97.8	97.2	93.1	91.6	90.4	89.7	89.2	88.5	87.8	86.8
C2048sD7	136.3	110.3	105.1	102.4	100.5	99.1	98.0	97.0	96.2	95.5	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
C2304sA7	115.1	99.7	95.7	93.9	93.8	93.6	93.3	92.8	92.0	91.2	90.6	87.2	85.5	84.3	83.4	82.7	82.0	79.4	77.6
C2304sB7	120.6	105.3	101.4	99.7	99.6	99.8	99.9	99.6	98.8	98.1	97.4	93.2	91.6	90.4	89.6	88.9	88.4	87.8	86.9
C2304sC7	120.6	105.3	101.4	99.7	99.6	99.8	99.9	99.6	98.8	98.1	97.4	93.2	91.6	90.4	89.6	88.9	88.4	87.8	86.8
C2304sD7	136.6	110.8	105.6	102.9	101.0	99.5	98.4	97.4	96.6	95.9	95.3	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0

Table IV.2/G.991.2 – STU-C side/asymmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	20	40	60	80	100	150	200	250	300	350	400	500	600	700	800	1000	1200	1400
C2048aA2	115.0	95.8	93.9	93.5	92.1	90.7	87.2	85.5	84.2	83.2	82.3	81.5	80.3	79.4	78.4	77.6	76.1	79.0	85.6
C2048aC2	120.6	101.6	99.8	100.1	99.0	97.5	93.2	91.5	90.2	89.1	88.2	87.5	86.5	87.7	87.6	86.8	85.3	87.9	93.8
C2048aD2	136.6	105.8	101.2	98.6	96.7	95.3	92.8	91.0	89.8	88.8	88.1	87.6	87.9	93.1	101.7	110.3	126.3	138.0	138.0
C2304aA2	115.0	95.8	94.0	93.8	92.5	91.1	87.5	85.7	84.4	83.4	82.5	81.8	80.4	79.4	78.4	77.6	76.1	79.0	85.6
C2304aC2	120.6	101.6	100.0	100.9	100.1	98.7	93.7	92.0	90.6	89.6	88.7	87.9	86.6	87.6	87.6	86.8	85.3	87.9	93.8
C2304aD2	137.5	107.5	102.9	100.3	98.5	97.0	94.5	92.8	91.5	90.5	89.7	89.1	88.7	92.0	99.6	107.6	122.5	135.2	138.0
C2048aD3	136.6	105.7	101.1	98.5	96.6	95.2	92.7	91.0	89.8	88.8	88.1	87.6	87.9	93.1	101.7	110.3	126.3	138.0	138.0
C2304aD3	137.5	107.4	102.8	100.2	98.3	96.9	94.4	92.7	91.5	90.5	89.7	89.1	88.7	92.0	99.6	107.6	122.5	135.2	138.0
C2048aA4	114.9	95.7	93.8	93.4	92.0	90.6	87.2	85.5	84.2	83.2	82.3	81.5	80.3	79.4	78.4	77.6	76.1	79.0	85.6

Table IV.2/G.991.2 – STU-C side/asymmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																		
	1	**20**	**40**	**60**	**80**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**500**	**600**	**700**	**800**	**1000**	**1200**	**1400**
C2048aC4	120.6	101.5	99.7	100.0	98.8	97.4	93.2	91.5	90.1	89.1	88.2	87.5	86.5	87.7	87.6	86.8	85.3	87.9	93.8
C2304aA4	115.0	95.7	93.9	93.6	92.3	90.9	87.4	85.7	84.4	83.4	82.5	81.8	80.4	79.4	78.4	77.6	76.1	79.0	85.6
C2304aC4	120.6	101.5	99.9	100.8	99.9	98.5	93.7	92.0	90.6	89.6	88.7	87.9	86.6	87.6	87.6	86.8	85.3	87.9	93.8
C2048aB5	120.4	101.1	99.2	99.3	98.2	97.0	93.1	91.4	90.1	89.1	88.2	87.5	86.5	87.7	87.7	86.9	85.4	88.2	94.5
C2304aB5	120.4	101.1	99.3	99.9	99.1	97.9	93.5	91.9	90.6	89.5	88.7	87.9	86.6	87.6	87.7	86.9	85.4	88.2	94.5
C2048aA6	115.2	95.8	94.0	93.6	92.3	90.9	87.3	85.5	84.2	83.2	82.3	81.5	80.3	79.4	78.4	77.6	76.1	79.0	85.6
C2048aC6	120.6	101.6	99.8	100.2	99.1	97.6	93.2	91.5	90.2	89.1	88.2	87.5	86.5	87.7	87.6	86.8	85.3	87.9	93.8
C2304aA6	115.4	96.0	94.1	94.0	92.8	91.3	87.5	85.7	84.5	83.4	82.5	81.8	80.4	79.4	78.4	77.6	76.1	79.0	85.6
C2304aC6	120.7	101.6	100.0	101.1	100.3	98.8	93.7	92.0	90.6	89.6	88.7	87.9	86.6	87.6	87.6	86.8	85.3	87.9	93.8
C2048aA7	115.0	95.7	93.8	93.4	92.1	90.7	87.2	85.5	84.2	83.2	82.3	81.5	80.3	79.4	78.4	77.6	76.1	79.0	85.6
C2048aB7	120.6	101.5	99.7	100.1	98.9	97.5	93.2	91.5	90.2	89.1	88.2	87.5	86.5	87.7	87.7	86.9	85.4	88.2	94.5
C2048aC7	120.6	101.5	99.7	100.1	98.9	97.5	93.2	91.5	90.2	89.1	88.2	87.5	86.5	87.7	87.6	86.8	85.3	87.9	93.8
C2048aD7	136.6	105.7	101.1	98.5	96.7	95.3	92.7	91.0	89.8	88.8	88.1	87.6	87.9	93.1	101.7	110.3	126.3	138.0	138.0
C2304aA7	115.1	95.8	93.9	93.7	92.4	91.0	87.5	85.7	84.4	83.4	82.5	81.8	80.4	79.4	78.4	77.6	76.1	79.0	85.6
C2304aB7	120.6	101.5	99.9	100.9	100.0	98.6	93.7	92.0	90.6	89.6	88.7	87.9	86.6	87.6	87.7	86.9	85.4	88.2	94.5
C2304aC7	120.6	101.5	99.9	100.9	100.0	98.6	93.7	92.0	90.6	89.6	88.7	87.9	86.6	87.6	87.6	86.8	85.3	87.9	93.8
C2304aD7	137.5	107.4	102.8	100.2	98.4	97.0	94.5	92.7	91.5	90.5	89.7	89.1	88.7	92.0	99.6	107.6	122.5	135.2	138.0

Table IV.3/G.991.2 – STU-R side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
R384sA2	114.9	99.2	95.3	93.7	92.6	92.1	92.3	92.4	91.8	91.0	90.4	87.9	86.2	84.8	87.3	93.1	98.1	123.1	115.4
R384sC2	120.6	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R384sD2	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R512sA2	114.9	99.4	95.7	94.1	92.9	92.1	91.6	91.1	90.9	90.8	90.4	87.9	86.2	84.8	87.3	93.1	98.1	122.5	115.4
R512sC2	120.6	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.4	96.5	96.1	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R512sD2	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R768sA2	114.9	99.6	96.0	94.5	93.4	92.6	91.9	91.0	90.4	89.8	89.3	87.9	86.1	84.8	87.3	93.0	98.0	117.7	114.9
R768sC2	120.6	105.2	101.0	98.9	98.1	97.5	96.9	96.3	95.6	95.1	94.7	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R768sD2	134.2	107.3	102.2	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
R1024sA2	114.9	99.7	96.1	94.7	93.7	92.9	92.2	91.3	90.6	89.9	89.3	87.4	86.1	84.8	87.3	93.0	97.8	113.4	113.5
R1024sC2	120.6	105.3	101.2	99.1	98.5	97.9	97.3	96.7	95.9	95.3	94.7	93.5	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R1024sD2	135.0	108.5	103.3	100.6	98.8	97.5	96.4	95.5	94.9	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
R1280sA2	114.9	99.7	96.1	94.8	93.9	93.1	92.5	91.6	90.8	90.1	89.5	87.2	85.9	84.7	87.2	92.8	97.4	108.6	110.3
R1280sC2	120.6	105.4	101.3	99.2	98.7	98.2	97.7	97.1	96.2	95.5	94.9	93.2	92.8	92.1	94.8	99.7	101.5	99.8	96.9
R1280sD2	135.7	109.4	104.3	101.5	99.7	98.3	97.2	96.3	95.5	94.9	94.4	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
R1536sA2	115.0	99.7	96.1	94.9	94.0	93.3	92.6	91.7	90.9	90.2	89.6	87.2	85.6	84.6	87.1	92.6	96.8	104.4	106.2
R1536sC2	120.6	105.4	101.3	99.3	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.3	92.4	91.8	94.7	99.6	101.4	99.8	96.9
R1536sD2	136.1	110.2	105.0	102.3	100.4	99.0	97.9	96.9	96.1	95.5	94.9	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0
R2048sA2	115.0	99.7	96.1	94.8	94.0	93.2	92.6	91.7	90.9	90.1	89.5	87.1	85.4	84.2	86.2	90.4	94.7	100.6	102.0
R2048sC2	120.6	105.4	101.3	99.3	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.1	92.0	91.0	92.6	96.2	100.1	99.7	96.9
R2048sD2	136.3	110.4	105.2	102.5	100.6	99.1	98.0	97.0	96.2	95.5	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
R2304sA2	115.0	99.7	96.1	94.8	94.0	93.3	92.7	91.8	90.9	90.2	89.6	87.1	85.4	84.1	85.8	88.5	91.3	98.0	99.1
R2304sC2	120.6	105.4	101.3	99.3	98.8	98.4	98.0	97.5	96.6	95.9	95.2	93.2	92.0	90.9	92.2	93.9	96.7	99.7	96.8
R2304sD2	136.6	110.9	105.7	102.9	101.0	99.6	98.4	97.4	96.6	95.9	95.3	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0

Table IV.3/G.991.2 – STU-R side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	10	20	30	40	50	60	70	80	90	100	150	200	250	300	350	400	600	800
R384sD3	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R512sD3	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R768sD3	134.1	107.3	102.2	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
R1024sD3	135.0	108.5	103.3	100.6	98.8	97.4	96.4	95.5	94.8	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
R1280sD3	135.6	109.4	104.2	101.5	99.7	98.3	97.2	96.2	95.5	94.9	94.3	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
R1536sD3	136.1	110.1	105.0	102.3	100.4	99.0	97.8	96.9	96.1	95.4	94.8	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0
R2048sD3	136.3	110.3	105.2	102.4	100.5	99.1	97.9	96.9	96.1	95.4	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
R2304sD3	136.6	110.8	105.6	102.9	101.0	99.5	98.3	97.4	96.5	95.8	95.2	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0
R384sA4	114.9	99.2	95.3	93.7	92.6	92.1	92.3	92.4	91.8	91.0	90.4	87.9	86.2	84.8	87.3	93.1	98.1	123.1	115.4
R384sC4	120.6	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R512sA4	114.9	99.4	95.6	94.0	92.9	92.1	91.6	91.0	90.9	90.8	90.4	87.9	86.2	84.8	87.3	93.1	98.1	122.8	115.4
R512sC4	120.6	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.4	96.5	96.1	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R768sA4	114.9	99.5	95.9	94.5	93.4	92.6	91.9	91.0	90.3	89.8	89.3	87.9	86.1	84.8	87.3	93.0	98.0	119.3	115.2
R768sC4	120.6	105.2	101.0	98.9	98.1	97.5	96.9	96.3	95.6	95.1	94.7	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R1024sA4	114.9	99.6	96.1	94.7	93.7	92.9	92.2	91.3	90.5	89.9	89.3	87.4	86.1	84.8	87.3	93.0	97.9	115.1	114.3
R1024sC4	120.6	105.3	101.2	99.1	98.5	97.9	97.3	96.7	95.9	95.3	94.7	93.5	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R1280sA4	114.9	99.6	96.1	94.8	93.9	93.1	92.4	91.5	90.7	90.0	89.4	87.2	85.9	84.7	87.2	92.9	97.5	110.0	111.6
R1280sC4	120.6	105.3	101.2	99.2	98.7	98.1	97.6	97.0	96.2	95.5	94.9	93.2	92.8	92.1	94.8	99.7	101.5	99.8	96.9
R1536sA4	114.9	99.6	96.1	94.8	93.9	93.2	92.6	91.7	90.8	90.1	89.5	87.2	85.6	84.6	87.1	92.6	96.9	105.5	107.7
R1536sC4	120.6	105.3	101.3	99.3	98.8	98.3	97.9	97.3	96.4	95.7	95.1	93.2	92.4	91.8	94.7	99.6	101.4	99.8	96.9
R2048sA4	115.0	99.6	96.0	94.7	93.9	93.1	92.5	91.6	90.8	90.1	89.4	87.0	85.4	84.2	86.1	90.4	94.6	100.8	102.6
R2048sC4	120.6	105.3	101.2	99.2	98.7	98.3	97.9	97.3	96.4	95.7	95.0	93.1	92.0	91.0	92.6	96.2	100.1	99.8	96.9
R2304sA4	115.0	99.6	96.0	94.7	93.9	93.2	92.6	91.7	90.8	90.1	89.5	87.0	85.3	84.1	85.8	88.4	91.2	98.1	99.5
R2304sC4	120.6	105.3	101.2	99.2	98.8	98.4	98.0	97.4	96.6	95.8	95.2	93.2	92.0	90.9	92.1	93.9	96.7	99.7	96.8

Table IV.3/G.991.2 – STU-R side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	10	20	30	40	50	60	70	80	90	100	150	200	250	300	350	400	600	800
R384sB5	120.4	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	93.9	98.2	102.0	129.0	121.3
R512sB5	120.4	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.3	96.5	96.1	94.4	93.4	92.1	93.9	98.2	102.0	129.0	121.3
R768sB5	120.4	105.1	100.9	98.8	98.0	97.4	96.8	96.3	95.6	95.1	94.7	94.4	93.4	92.1	93.9	98.2	102.0	128.7	121.3
R1024sB5	120.4	105.2	101.1	99.0	98.3	97.8	97.2	96.6	95.9	95.2	94.7	93.5	93.4	92.1	93.9	98.2	102.0	128.1	121.3
R1280sB5	120.4	105.2	101.1	99.0	98.5	98.0	97.5	96.9	96.1	95.5	94.8	93.2	92.8	92.1	93.9	98.2	101.9	126.1	121.2
R1536sB5	120.4	105.1	101.1	99.0	98.6	98.1	97.7	97.2	96.3	95.6	95.0	93.2	92.3	91.8	93.8	98.2	101.9	122.8	120.8
R2048sB5	120.4	105.0	100.9	98.9	98.4	98.0	97.6	97.1	96.2	95.5	94.9	93.0	91.9	90.9	92.2	95.7	100.2	115.8	118.4
R2304sB5	120.5	104.9	100.9	98.8	98.4	98.0	97.7	97.2	96.3	95.6	95.0	93.0	91.9	90.9	91.7	93.6	96.7	111.7	115.7
R384sA6	114.9	99.2	95.3	93.7	92.6	92.1	92.3	92.4	91.8	91.0	90.4	87.9	86.2	84.8	87.3	93.1	98.1	122.6	115.4
R384sC6	120.6	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R512sA6	114.9	99.4	95.6	94.1	92.9	92.1	91.6	91.1	90.9	90.8	90.4	87.9	86.2	84.8	87.3	93.1	98.0	120.2	115.2
R512sC6	120.6	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.4	96.5	96.1	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R768sA6	114.9	99.6	95.9	94.5	93.4	92.6	91.9	91.1	90.4	89.8	89.3	87.9	86.1	84.8	87.3	93.0	97.8	111.7	112.2
R768sC6	120.6	105.2	101.0	98.9	98.1	97.5	96.9	96.3	95.6	95.1	94.7	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R1024sA6	115.0	99.7	96.1	94.7	93.8	92.9	92.3	91.4	90.6	89.9	89.4	87.4	86.1	84.8	87.3	92.8	97.3	106.6	107.9
R1024sC6	120.6	105.3	101.2	99.1	98.5	97.9	97.3	96.7	96.0	95.3	94.7	93.5	93.4	92.1	94.8	99.7	101.4	99.8	96.9
R1280sA6	115.0	99.7	96.1	94.9	93.9	93.2	92.5	91.6	90.8	90.1	89.5	87.2	85.8	84.7	87.2	92.6	96.7	102.9	103.8
R1280sC6	120.6	105.4	101.2	99.2	98.7	98.2	97.7	97.1	96.3	95.5	94.9	93.2	92.8	92.1	94.8	99.6	101.3	99.8	96.9
R1536sA6	115.1	99.8	96.2	94.9	94.1	93.3	92.7	91.8	91.0	90.3	89.6	87.2	85.6	84.6	87.2	92.2	95.8	99.6	100.5
R1536sC6	120.6	105.4	101.3	99.3	98.8	98.4	97.9	97.3	96.5	95.8	95.1	93.2	92.3	91.8	94.7	99.5	101.2	99.7	96.9
R2048sA6	115.4	100.0	96.3	94.9	94.1	93.3	92.7	91.8	91.0	90.3	89.6	87.1	85.4	84.3	86.3	90.0	93.5	96.1	95.8
R2048sC6	120.7	105.4	101.3	99.3	98.8	98.4	98.0	97.4	96.5	95.8	95.1	93.1	91.9	91.0	92.6	96.1	99.9	99.6	96.8
R2304sA6	115.6	100.2	96.4	95.0	94.2	93.4	92.8	91.9	91.1	90.4	89.7	87.1	85.4	84.3	86.0	88.3	90.8	93.8	93.8
R2304sC6	120.7	105.4	101.3	99.3	98.9	98.5	98.1	97.5	96.7	95.9	95.2	93.2	92.0	91.0	92.2	93.8	96.6	99.4	96.7

Table IV.3/G.991.2 – STU-R side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
R384sA7	114.9	99.2	95.3	93.7	92.6	92.1	92.3	92.4	91.8	91.0	90.4	87.9	86.2	84.8	87.3	93.1	98.1	123.1	115.4
R384sB7	120.6	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	93.9	98.2	102.0	129.0	121.3
R384sC7	120.6	104.6	100.2	98.1	97.3	96.9	97.3	98.2	97.6	96.9	96.2	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R384sD7	131.8	104.4	99.5	97.1	95.8	95.3	96.4	100.5	107.0	114.2	121.6	138.0	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R512sA7	114.9	99.4	95.6	94.0	92.9	92.1	91.6	91.0	90.9	90.8	90.4	87.9	86.2	84.8	87.3	93.1	98.1	122.9	115.4
R512sB7	120.6	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.4	96.5	96.1	94.4	93.4	92.1	93.9	98.2	102.0	129.0	121.3
R512sC7	120.6	104.9	100.6	98.4	97.6	96.9	96.5	96.3	96.4	96.5	96.1	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R512sD7	132.8	105.6	100.6	98.0	96.4	95.4	94.8	94.8	95.8	98.7	103.2	131.4	138.0	138.0	138.0	138.0	138.0	138.0	138.0
R768sA7	114.9	99.5	95.9	94.5	93.4	92.6	91.9	91.0	90.3	89.8	89.3	87.9	86.1	84.8	87.3	93.1	98.0	120.5	115.3
R768sB7	120.6	105.2	101.0	98.9	98.1	97.5	96.9	96.3	95.6	95.1	94.7	94.4	93.4	92.1	93.9	98.2	102.0	128.8	121.3
R768sC7	120.6	105.2	101.0	98.9	98.1	97.5	96.9	96.3	95.6	95.1	94.7	94.4	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R768sD7	134.1	107.2	102.1	99.5	97.7	96.5	95.5	94.8	94.3	93.9	93.8	102.6	120.9	138.0	138.0	138.0	138.0	138.0	138.0
R1024sA7	114.9	99.6	96.0	94.7	93.7	92.9	92.2	91.3	90.6	89.9	89.3	87.4	86.1	84.8	87.3	93.0	97.9	117.3	114.8
R1024sB7	120.6	105.3	101.2	99.1	98.5	97.9	97.3	96.7	95.9	95.3	94.7	93.5	93.4	92.1	93.9	98.2	102.0	128.3	121.3
R1024sC7	120.6	105.3	101.2	99.1	98.5	97.9	97.3	96.7	95.9	95.3	94.7	93.5	93.4	92.1	94.8	99.7	101.5	99.8	96.9
R1024sD7	135.0	108.4	103.3	100.6	98.8	97.4	96.4	95.5	94.9	94.3	93.9	93.6	102.1	115.8	130.8	138.0	138.0	138.0	138.0
R1280sA7	114.9	99.6	96.1	94.8	93.9	93.1	92.5	91.5	90.8	90.1	89.5	87.2	85.9	84.8	87.3	92.9	97.7	113.2	113.3
R1280sB7	120.6	105.3	101.2	99.2	98.7	98.1	97.7	97.1	96.2	95.5	94.9	93.2	92.8	92.1	93.9	98.2	101.9	127.0	121.2
R1280sC7	120.6	105.3	101.2	99.2	98.7	98.1	97.7	97.1	96.2	95.5	94.9	93.2	92.8	92.1	94.8	99.7	101.5	99.8	96.9
R1280sD7	135.7	109.4	104.2	101.5	99.7	98.3	97.2	96.3	95.5	94.9	94.3	92.8	94.0	101.7	112.6	124.2	136.9	138.0	138.0
R1536sA7	115.0	99.7	96.1	94.8	93.9	93.2	92.6	91.7	90.9	90.2	89.6	87.2	85.6	84.6	87.2	92.8	97.3	108.8	110.3
R1536sB7	120.6	105.3	101.3	99.3	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.2	92.4	91.8	93.9	98.2	101.9	124.9	121.0
R1536sC7	120.6	105.3	101.3	99.3	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.2	92.4	91.8	94.7	99.6	101.4	99.8	96.9
R1536sD7	136.1	110.1	105.0	102.2	100.4	99.0	97.8	96.9	96.1	95.5	94.9	92.9	92.3	94.4	101.4	110.4	119.9	138.0	138.0

Table IV.3/G.991.2 – STU-R side/symmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**600**	**800**
R2048sA7	115.0	99.7	96.0	94.7	93.9	93.2	92.6	91.7	90.8	90.1	89.5	87.1	85.4	84.2	86.2	90.6	95.4	104.5	106.2
R2048sB7	120.6	105.3	101.2	99.2	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.1	92.0	91.0	92.2	95.8	100.4	121.1	120.2
R2048sC7	120.6	105.3	101.2	99.2	98.8	98.3	97.9	97.3	96.5	95.7	95.1	93.1	92.0	91.0	92.6	96.3	100.2	99.8	96.9
R2048sD7	136.3	110.3	105.1	102.4	100.5	99.1	98.0	97.0	96.2	95.5	94.8	92.6	91.3	90.7	91.2	94.1	99.8	128.9	138.0
R2304sA7	115.1	99.7	96.1	94.8	93.9	93.2	92.6	91.7	90.9	90.2	89.6	87.1	85.4	84.2	86.0	88.7	91.8	102.1	103.6
R2304sB7	120.6	105.3	101.2	99.2	98.8	98.4	98.0	97.5	96.6	95.9	95.2	93.2	92.0	91.0	91.8	93.7	96.9	116.6	118.9
R2304sC7	120.6	105.3	101.2	99.2	98.8	98.4	98.0	97.5	96.6	95.9	95.2	93.2	92.0	91.0	92.2	93.9	96.8	99.8	96.9
R2304sD7	136.6	110.8	105.6	102.9	101.0	99.5	98.4	97.4	96.6	95.9	95.3	92.9	91.5	90.7	90.4	91.3	94.4	118.1	138.0

Table IV.4/G.991.2 – STU-R side/asymmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**20**	**40**	**60**	**80**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**500**	**600**	**700**	**800**	**1000**	**1200**	**1400**
R2048aA2	115.0	96.0	93.6	92.0	90.3	88.9	86.5	84.9	83.8	85.4	89.5	94.8	100.7	103.2	104.0	105.0	107.4	113.3	121.7
R2048aC2	120.6	101.1	98.4	97.2	95.6	94.2	92.2	91.0	90.1	91.2	94.8	99.8	101.7	99.8	98.0	96.9	95.5	97.3	99.6
R2048aD2	135.1	103.3	98.6	96.0	94.2	92.9	90.6	89.3	88.7	89.0	92.2	98.9	113.0	124.8	134.6	137.6	138.0	138.0	138.0
R2304aA2	115.0	96.1	93.9	92.6	90.8	89.4	87.0	85.3	84.1	85.6	87.9	91.2	97.7	99.6	100.2	101.0	102.6	108.2	116.8
R2304aC2	120.6	101.3	98.8	97.8	96.4	95.0	93.0	91.8	90.7	91.6	93.1	96.4	101.5	99.7	98.0	96.9	95.5	97.3	99.6
R2304aD2	136.2	105.0	100.4	97.8	95.9	94.6	92.2	90.8	89.9	89.6	90.4	93.8	106.4	118.0	129.7	136.4	138.0	138.0	138.0
R2048aD3	135.1	103.3	98.6	96.0	94.2	92.9	90.6	89.3	88.7	89.0	92.2	98.9	113.1	125.2	135.0	137.7	138.0	138.0	138.0
R2304aD3	136.2	105.0	100.3	97.7	95.9	94.5	92.2	90.8	89.9	89.6	90.4	93.8	106.4	118.2	130.1	136.6	138.0	138.0	138.0
R2048aA4	114.9	95.9	93.5	92.0	90.2	88.9	86.5	84.9	83.8	85.4	89.4	94.7	100.6	103.3	104.2	105.4	107.9	113.9	122.2
R2048aC4	120.6	101.1	98.4	97.1	95.6	94.2	92.2	91.0	90.1	91.2	94.8	99.8	101.7	99.8	98.0	96.9	95.5	97.3	99.6

Table IV.4/G.991.2 – STU-R side/asymmetric PSDs

Noise profile	Magnitude of the noise in dBm per Hz (sign is always negative) as a function of frequency in kHz																	
	1	**20**	**40**	**60**	**80**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**500**	**600**	**700**	**800**	**1000**	**1200**	**1400**
R2304aA4	115.0	96.0	93.8	92.5	90.7	89.4	86.9	85.2	84.0	85.6	87.9	91.0	97.5	99.4	100.2	101.0	102.8	108.4	117.1
R2304aC4	120.6	101.2	98.7	97.8	96.4	94.9	92.9	91.7	90.7	91.6	93.1	96.4	101.5	99.7	98.0	96.9	95.5	97.3	99.6
R2048aB5	120.4	100.8	98.1	96.9	95.5	94.1	92.1	90.9	90.0	90.9	94.5	99.9	109.9	117.5	117.8	119.3	124.5	128.9	132.5
R2304aB5	120.4	100.9	98.4	97.6	96.2	94.8	92.8	91.7	90.6	91.3	92.9	96.3	106.7	113.3	115.1	116.9	121.1	126.2	131.8
R2048aA6	115.2	96.0	93.7	92.1	90.4	89.0	86.5	84.9	83.8	85.5	89.3	94.0	100.2	99.1	100.6	99.6	100.0	105.0	112.9
R2048aC6	120.6	101.1	98.4	97.2	95.6	94.3	92.2	91.0	90.1	91.2	94.7	99.6	101.7	99.7	98.0	96.8	95.5	97.3	99.6
R2304aA6	115.4	96.3	94.0	92.7	90.9	89.6	87.0	85.3	84.1	85.7	87.7	90.6	96.6	95.4	97.3	95.4	94.9	99.4	106.7
R2304aC6	120.7	101.3	98.8	97.9	96.4	95.0	93.0	91.7	90.7	91.7	93.1	96.3	101.4	99.6	98.0	96.8	95.5	97.3	99.6
R2048aA7	115.0	95.9	93.5	92.0	90.3	88.9	86.5	84.9	83.8	85.5	89.6	95.2	102.5	106.9	107.0	108.3	110.8	116.4	124.1
R2048aB7	120.6	101.1	98.4	97.1	95.6	94.2	92.2	91.0	90.1	91.0	94.5	100.1	111.2	122.3	119.5	120.5	125.9	129.7	132.6
R2048aC7	120.6	101.1	98.4	97.1	95.6	94.2	92.2	91.0	90.1	91.2	94.8	99.8	101.8	99.8	98.1	96.9	95.5	97.3	99.6
R2048aD7	135.1	103.3	98.6	96.0	94.2	92.9	90.6	89.3	88.7	89.0	92.2	98.9	113.6	127.0	135.9	137.8	138.0	138.0	138.0
R2304aA7	115.1	96.0	93.8	92.5	90.8	89.4	87.0	85.3	84.1	85.7	88.1	91.4	99.8	102.7	103.2	104.5	105.8	111.3	119.7
R2304aB7	120.6	101.2	98.7	97.8	96.4	95.0	92.9	91.7	90.7	91.4	93.0	96.5	108.3	118.2	118.3	119.4	124.0	128.5	132.3
R2304aC7	120.6	101.2	98.7	97.8	96.4	95.0	92.9	91.7	90.7	91.7	93.1	96.4	101.6	99.8	98.0	96.9	95.5	97.3	99.6
R2304aD7	136.2	105.0	100.3	97.7	95.9	94.6	92.2	90.8	89.9	89.6	90.4	93.9	106.7	119.4	131.9	137.2	138.0	138.0	138.0

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